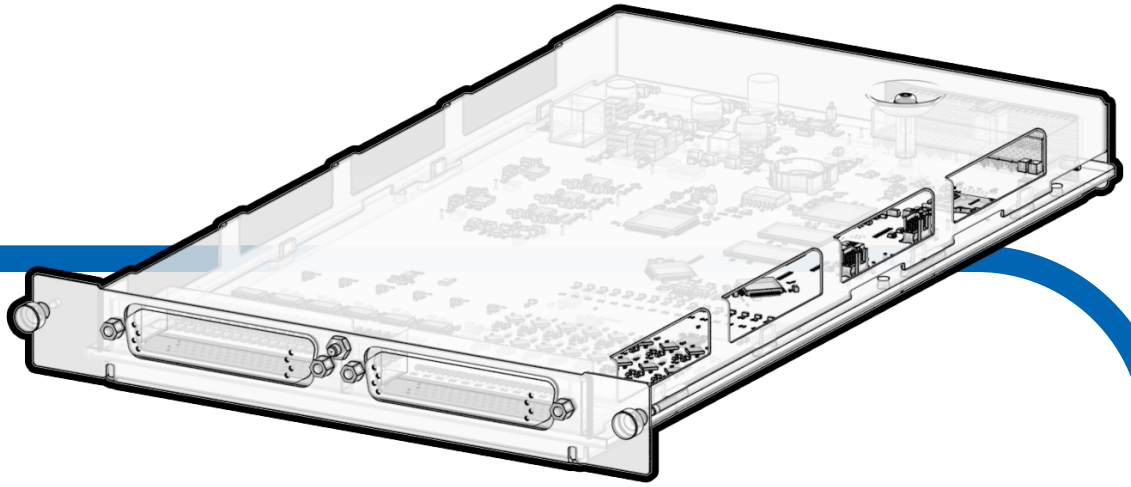
Datasheet



DE2110

Multifunction I/O Module

32 AI (16 DIFF), 16 AO, 48 DIO

DEICO

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Contents

1. Description

DE2110 is a fully integrated digital and analog I/O system. This system provides 48 digital I/O, 32 single-ended or 16 differential analog inputs, and 16 analog output channels. All I/O channels are routed to the rear panel through two separate DB-78 connectors. The module includes a flexible digital I/O system that can interface with multiple logic families and all digital channels feature a programmable threshold level.

The DE2110 features an 18-bit, simultaneous sampling, analog-to-digital data acquisition system (DAS) that is configurable for 32 single-ended or 16 differential channels. Each input channel is equipped with analog clamp protection.

The module also provides a 16-channel, 16-bit analog output stage with a precision reference. Each output is independently programmable to a range of ±15 V. The analog outputs are guaranteed monotonic and include built-in rail-to-rail buffers capable of sourcing or sinking up to 55 mA. These outputs can be automatically calibrated using the integrated ADC block.

1.1. Key Features

Connectivity

- Standard 10/100 base-t ethernet interface
- USB 1.1 full-speed interface (12 Mb/s)

Robustness and Reliability

- Fully protected analog and digital I/O lines
- MTBF (Mean Time Between Failures) exceeding 150,000 hours
- ESD (Electrostatic Discharge) protection up to 7 kV

Operational Flexibility

- Supports PC-based, standalone, or embedded controller operation
- LXI Class C compliant for system integration

Standards and Compliance

- The DE2110 is fully compliant with the following standards for safety, emissions, and immunity:
  - Environmental: IEC 60068-2-1, IEC 60068-2-2, IEC 60068-2-27, IEC 60068-2-64, IEC 60068-2-78
  - EMC/EMI: EN 61326, EN 55011 (CISPR 11), AS/NZS CISPR 11, FCC 47 CFR Part 15B, ICES-001

Typical Applications

The DE2110 is ideal for a wide range of demanding applications, including:

- High-density measurement and sensing
- Data Acquisition (DAQ) systems
- Instrumentation and control systems
- Automated Test Equipment (ATE)
- Process control and industrial automation
- Hardware-in-the-Loop (HIL) simulation

1.1.1. Analog Input

Features an 18-bit, simultaneous-sampling, Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC).

Channel Configuration

- 32 single-ended channels
- 16 differential channels

Performance

- Sampling rate: 1 MS/s (megasample per second)
- Selectable bandwidth: 2 kHz and 220 kHz (per channel)

Input Ranges (per-channel selectable)

- Bipolar single-ended: ±12.5 V, ±10 V, ±6.25 V, ±5 V, ±2.5 V
- Unipolar single-ended: 0 V to 12.5 V, 0 V to 10 V, 0 V to 5 V
- Bipolar differential: ±20 V, ±12.5 V, ±10 V, ±5 V

Input Protection

- Input impedance: 1.2 MΩ
- ESD protection: ±6 kV
- Input clamp protection: ±21 V (up to ±48 V)

1.1.2. Analog Output

Features an 16-channel, 16-bit, Digital-to-Analog Converter (DAC) with an integrated precision reference.

Output Stage

- Guaranteed monotonic performance
- Integrated rail-to-rail output buffers
- Current drive: ±55 mA (source/sink)

Output Ranges (independently programmable per channel)

- Unipolar: 0 V to 5 V, 0 V to 10 V
- Bipolar: ±5 V, ±10 V, ±15 V

Performance and Accuracy

- Settling time: <15 µs
- Integral Non-Linearity (INL): ±3 LSB (max)
- Calibration: all channels feature automatic calibration using the internal ADC

1.1.3. Digital I/O

Features a high-speed, flexible digital I/O system designed for hardware-timed control and digital device testing.

Performance

- Data rate: up to 420 Mb/s
- Timing: precision hardware-timed control

Architecture

- Provides 6 bidirectional digital channels, with each channel consisting of 8 bit (48 bit total).
- Each channel's direction (input or output) is independently configurable.

Programmable Logic Levels

- The core feature is the programmable voltage thresholds, adjustable from 1.1 V to 5.25 V.
- This allows the module to directly interface with various logic families (e.g., TTL, CMOS, LVCMOS) without external level-shifting circuitry.
- Enables precise characterization of a Device Under Test's (DUT) input voltage thresholds (VIL, VIH), as illustrated in Figure 1.

Input/Output Characteristics

- Input buffers: All inputs feature Schmitt-trigger buffers for high noise immunity and reliable operation with slow-slewing or noisy signals
- Supported states: supports logic low (0), logic high (1), and high-impedance (Tri-state, Z) for advanced waveform generation and bus simulation
- Output Drive Capacity: 32 mA per channel
- Current Clamping: ±50 mA per channel

The programmable input (VIH, VIL) and output (VOH, VOL) voltage levels allow the DE2110 to interface directly with a wide range of devices.

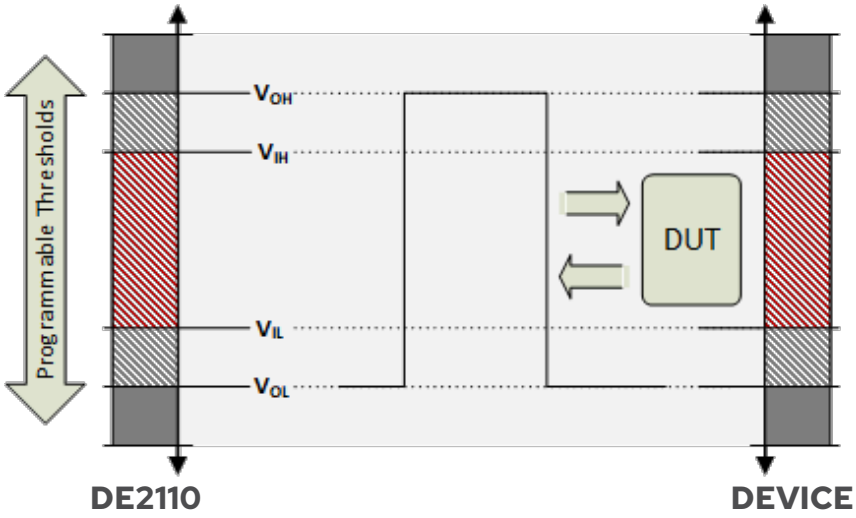

Figure 1: Flexible Digital I/O Interface with Programmable Thresholds

2. Hardware Overview

2.1. Circuitry

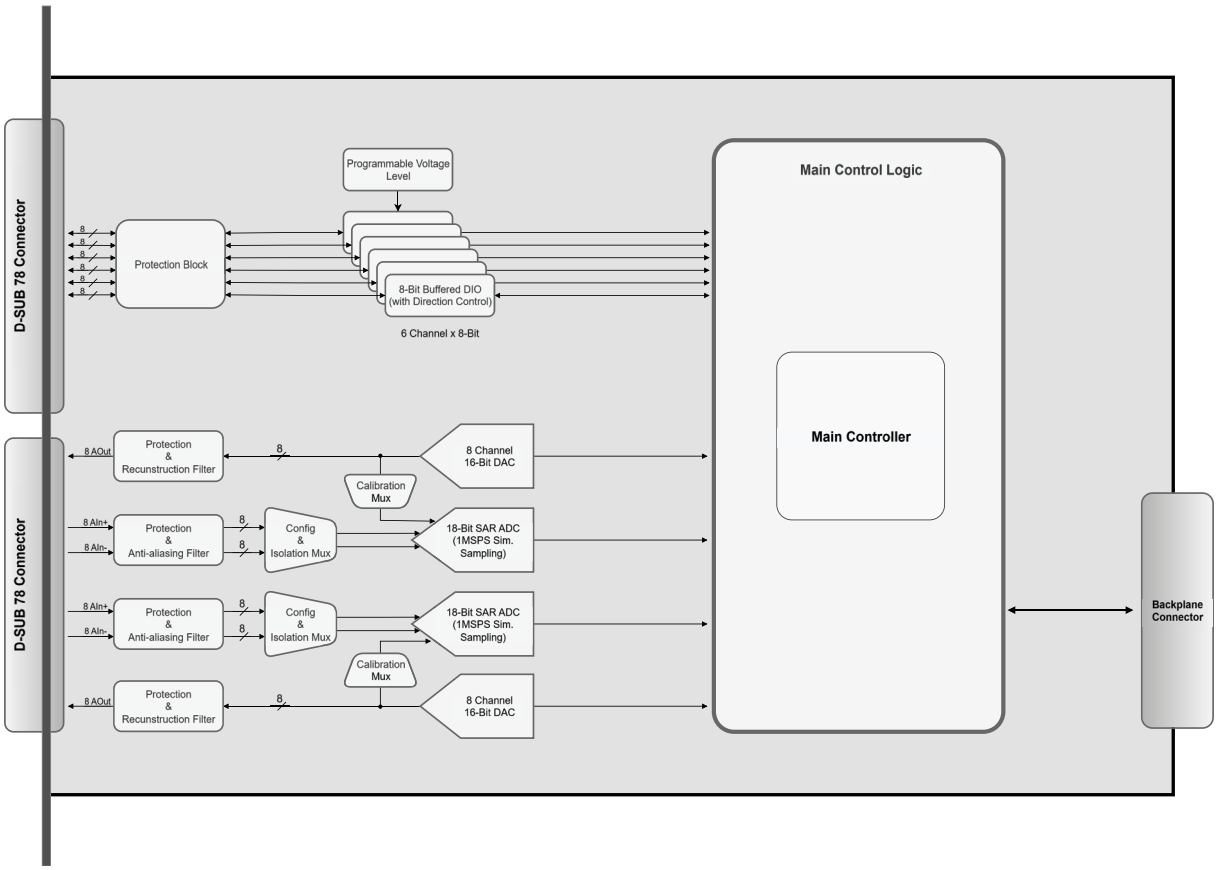

Figure 2: DE2110 Functional Block Diagram

2.2. Hardware Specifications

2.2.1. Electrical

Table 1: Electrical Specifications

Specification	Description
Input Voltage	+24 V DC (from backplane)
Power Consumption	Typical: 6 W Maximum: 32 W

Table 2: Analog Inputs

Specification	Description
Number of Channels	32 single-ended or 16 fully differential (software-selectable)
ADC Resolution / Architecture	18 bit / SAR (Successive Approximation Register)
Sampling Rate	1 MS/s (megasample per second)
Simultaneous Sampling	Differential: 16 channels Single-ended: 16 channels
Bandwidth	Selectable: 2 kHz and 220 kHz (per channel)
INL (Integral Non-Linearity)	±4 LSB (max)
DNL (Differential Non-Linearity)	±2 LSB (max)
Offset / Gain Error Drift	±0.5 ppm/°C (typical)
Input Ranges (per channel)	Bipolar single-ended: ±12.5 V, ±10 V, ±6.25 V, ±5 V, ±2.5 V Unipolar single-ended: 0 V to 12.5 V, 0 V to 10 V, 0 V to 5 V Bipolar differential: ±20 V, ±12.5 V, ±10 V, ±5 V
Input Impedance	1.2 MΩ
Protection	Input clamp: ±21 V (up to ±48 V) ESD (human body model): ±6 kV
Input Channel Control	Each channel can be programmatically disconnected (set to a high-impedance state) from the ADC input.

Table 3: Analog Outputs

Specification	Description
Number of channels	16
Resolution	Full 16-bit resolution at all ranges
Voltage Output Ranges	0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V, ±15 V (independently programmable output ranges)
Output Impedance	0.01 Ω
DAC Type	Voltage - buffered
INL Error	±3 LSB (max)
Outputs Drive Current	±55 mA (guaranteed)
Settling Time	<15 µs (to ±1 LSB at 16 bits)
Capacitive Load Driving	1000 pF
Voltage Output Slew Rate	> 3.5 V/µs
Output Current Limit	±115 mA
Gain Temperature Coefficient	2 ppm/°C
Protection	Resettable PTC fuse and ESD protection

Table 4: Digital I/O

Specification	Description
Threshold Voltage Accuracy	±10 mV (over 0 V to 5.25 V DC)
Total Number of Bits	48 (6 channel x 8 bit)
Number of Channels	6
Width per Channel	8 bit
Direction Control	Per-channel, independently configurable
Maximum Data Rate	420 Mb/s
Drive Capacity (per channel)	±32 mA (continuous)
Input Voltage Thresholds	Programmable, 0 V to 5.25 V
Output Voltage Levels	Programmable, 1.1 V to 5.25 V (supports open-drain configuration)
ESD Protection	±7 kV (human body model)
Current Clamping	±50 mA
Output Type	Tri-state, non-inverted
Input Type	Schmitt-trigger inputs allow for slow or noisy inputs

2.2.2. Physical

Table 5: Physical Specifications

Specification	Description
Dimensions (L x W x H)	281.5 mm x 180.1 mm x 25.7 mm
Weight	2 kg (typical)
Front Panel Connectors	2x D-SUB 78 (HARTING P/N: 09565527613)

2.2.3. Environmental

Table 6: Environmental Specifications

Specification	Condition	Value
Operating Humidity	Relative, non-condensing	10% - 90%
Storage Humidity	Relative, non-condensing	5% - 95%
Operating Temperature*	Forced-air cooling from chassis	0 °C to +55 °C
Storage Temperature	N/A (Not Applicable)	-40 °C to +71 °C

** The specified operating temperature range is only guaranteed when the module is installed in a chassis that provides adequate forced-air cooling.*

3. Software Overview

This module is compatible with IVISwtch class.

4. Signal Connections

This diagram outlines the integrated I/O architecture of the DE2110. On the digital side, the 48 I/O lines are grouped into six 8-bit “Channels” for ease of programming. On the analog side, the 32 single-ended / 16 differential inputs are managed by two 18-bit ADCs, while the 16 analog outputs are generated by two 16-bit DACs. This parallel and modular architecture ensures maximum flexibility and performance for both high-density digital testing and precision analog measurement and signal generation.

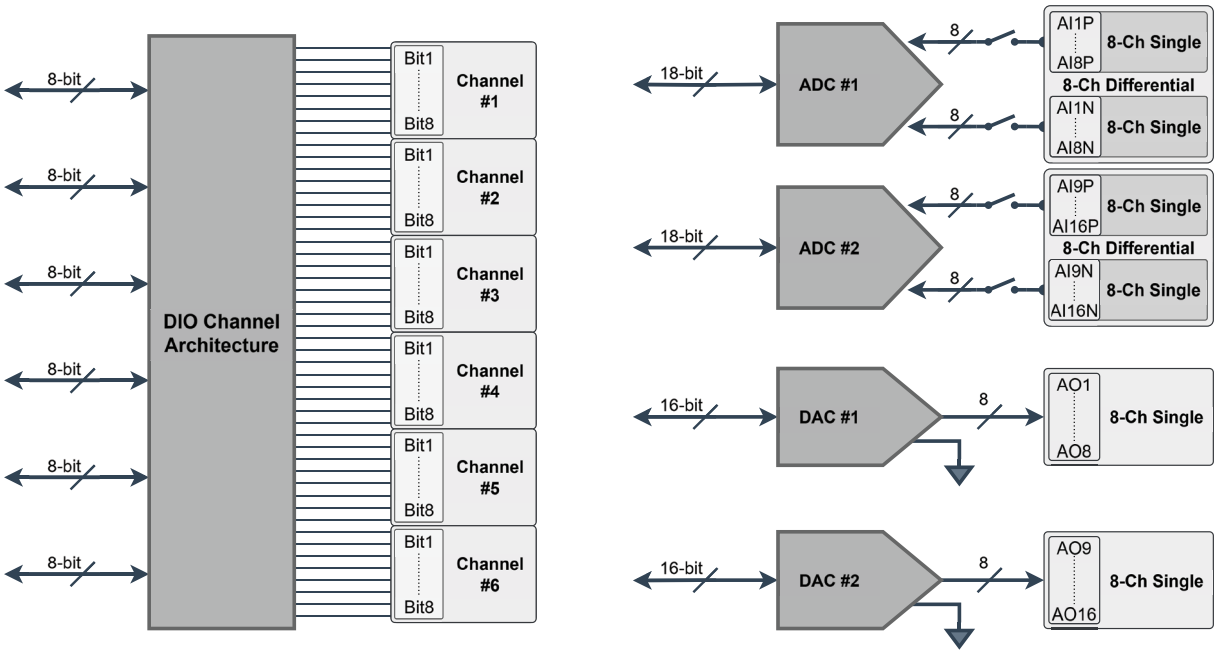

Figure 3: DE2110 I/O Channel Architecture

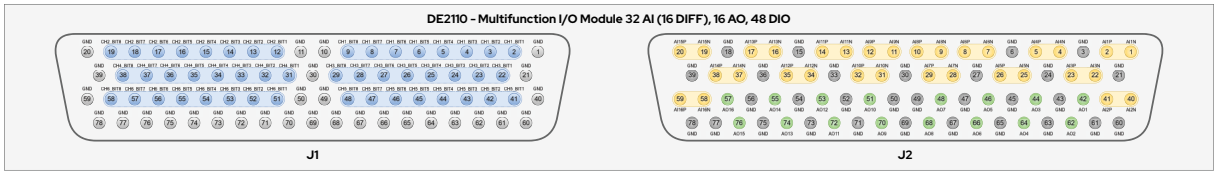

Figure 4 : Module Front Panel Connectors

4.1. Analog I/O Connector (J2, DB-78)

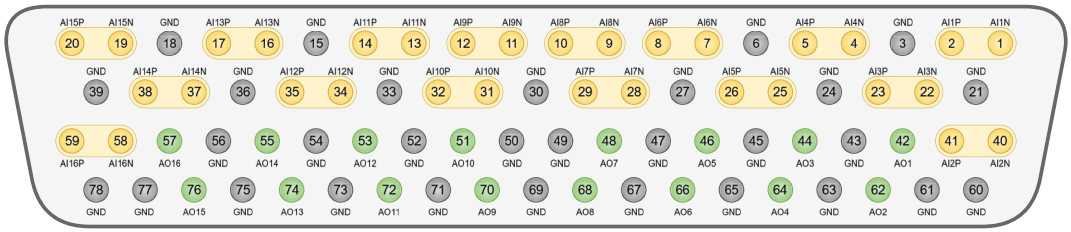

Figure 5 : Analog I/O Connector Pinout (J2, DB-78, Female)

Table 7: Analog I/O Connector Pin Assignments

Description		Pin	Description		Pin
Analog Input	AI1N / SE1	1	Analog Input	AI9N / SE17	11
	AI1P / SE2	2		AI9P / SE18	12
	AI2N / SE3	40		AI10N / SE19	31
	AI2P / SE4	41		AI10P / SE20	32
	AI3N / SE5	22		AI11N / SE21	13
	AI3P / SE6	23		AI11P / SE22	14
	AI4N / SE7	4		AI12N / SE23	34
	AI4P / SE8	5		AI12P / SE24	35
	AI5N / SE9	25		AI13N / SE25	16
	AI5P / SE10	26		AI13P / SE26	17
	AI6N / SE11	7		AI14N / SE27	37
	AI6P / SE12	8		AI14P / SE28	38
	AI7N / SE13	28		AI15N / SE29	19
	AI7P / SE14	29		AI15P / SE30	20
	AI8N / SE15	9		AI16N / SE31	58
	AI8P / SE16	10		AI16P / SE32	59
Analog Output	AO 1	42	Analog Output	AO 9	70
	AO 2	62		AO 10	51
	AO 3	44		AO 11	72
	AO 4	64		AO 12	53
	AO 5	46		AO 13	74
	AO 6	66		AO 14	55
	AO 7	48		AO 15	76
	AO 8	68		AO 16	57
GND		3	GND		50
		6			52
		15			54
		18			56
		21			60
		24			61
		27			63
		30			65
		33			67
		36			69
		39			71
		43			73
		45			75
		47			77
		49			78

4.2. Digital I/O Connector (J1, DB-78)

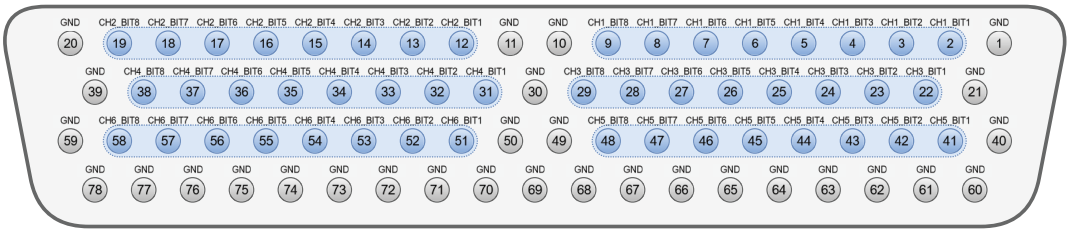

Figure 6 : Digital I/O Connector Pinout (J1, DB-78, Female)

Table 8: Digital I/O Connector Pin Assignments

Description		Pin	Description		Pin	Description		Pin	Description	Pin	Description	Pin
CH1	BIT1	2	CH3	BIT1	22	CH5	BIT1	41	GND	1	GND	65
	BIT2	3		BIT2	23		BIT2	42		10		66
	BIT3	4		BIT3	24		BIT3	43		11		67
	BIT4	5		BIT4	25		BIT4	44		20		68
	BIT5	6		BIT5	26		BIT5	45		21		69
	BIT6	7		BIT6	27		BIT6	46		30		70
	BIT7	8		BIT7	28		BIT7	47		39		71
	BIT8	9		BIT8	29		BIT8	48		40		72
CH2	BIT1	12	CH4	BIT1	31	CH6	BIT1	51		49		73
	BIT2	13		BIT2	32		BIT2	52		50		74
	BIT3	14		BIT3	33		BIT3	53		59		75
	BIT4	15		BIT4	34		BIT4	54		60		76
	BIT5	16		BIT5	35		BIT5	55		61		77
	BIT6	17		BIT6	36		BIT6	56		62		78
	BIT7	18		BIT7	37		BIT7	57		63		
	BIT8	19		BIT8	38		BIT8	58		64		

5. Safety Guidelines

Caution

The DE2110 shall not be operated in any manner not specified in this document. Misuse of the product may result in a hazard. Safety protection features may be compromised if the product is damaged. In the event of damage, the product shall be returned for repair.

6. Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC). These requirements and limits provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in some installations, if the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions specified in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by DEICO could void your authority to operate it under your local regulatory rules.

Caution

To ensure the specified EMC performance, the product shall be operated only with shielded cables and accessories.

Caution

To ensure the specified EMC performance, the length of any cable attached to the front connectors shall not exceed 3 m (10 ft.).

7. Supporting Products & Software

DE2110 should be used with Switching and DAQ Mainframe 8 Slot (DE2000) or Single Module Mainframe (DE2001).

Note

When the DE2110 is used with the DE2001, the ethernet speed shall be limited to 100 Mb/s.

Caution

The DE2110 shall not be operated without the DE2000 or DE2001. No connections shall be made to the rear panel connector.