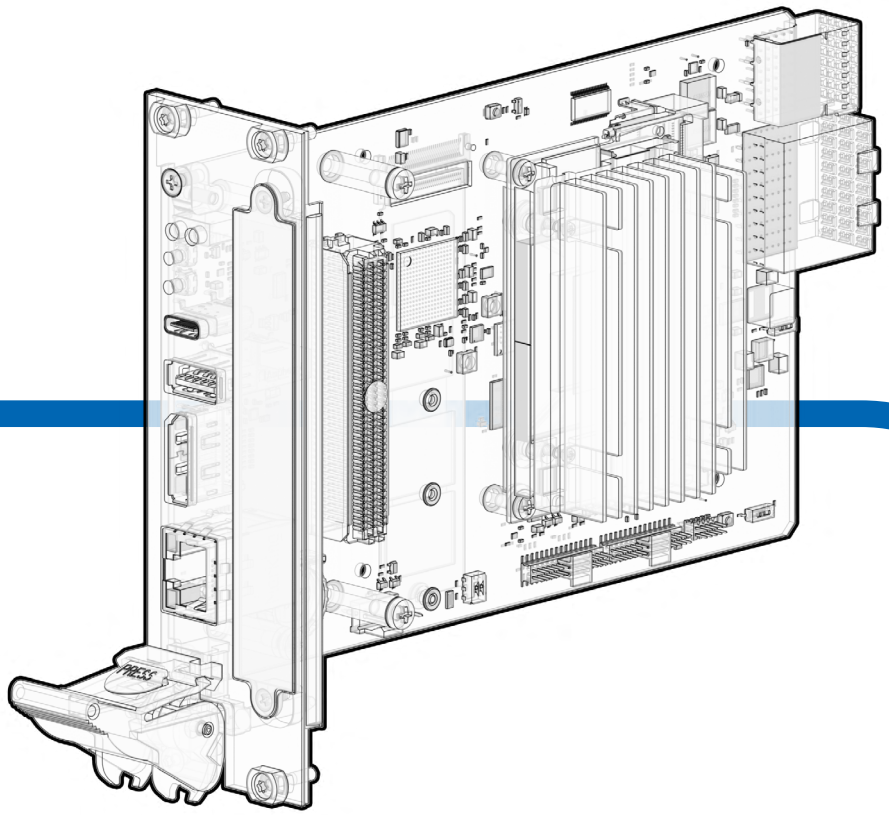
Datasheet



DE160202

PXIe Jetson Orin NX Module

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Contents

1. Description

DE160202 PXIe Jetson Orin NX Module is a high-performance and power-efficient edge AI platform, designed around NVIDIA's powerful Jetson Orin NX system-on-module (SoM) to deliver next-generation AI capabilities in a compact and modular form. By integrating this advanced SoM into the PXIe form factor, the module offers a scalable and robust solution for industries that require significant processing power in constrained environments.

A key feature of the PXIe Jetson Orin NX Module is its add-on board connector, which allows users to expand and customize the platform by adding add-on boards. This connector enables the integration of specialized hardware, such as GMSL2 and 3G-SDI interfaces, through custom-designed add-on boards. The signals for these high-bandwidth interfaces are routed directly from the Jetson platform, ensuring seamless communication and fast data transfer between the module and external sensors or devices.

This modular approach gives users the flexibility to tailor the system to specific project needs, adding new capabilities as required without redesigning the entire platform. The ability to add GMSL2 and 3G-SDI interfaces through add-on boards allows the system to handle high-bandwidth sensor data streams and video signals, making it ideal for applications in real-time video analytics, industrial automation, robotics, and advanced surveillance systems.

The PXIe Jetson Orin NX Module leverages a powerful GPU, deep learning accelerators, and a high-performance ARM CPU to run modern AI models efficiently at the edge. This enables rapid, real-time decision-making with low latency, reducing the dependency on cloud connectivity and ensuring reliable performance in critical applications.

1.1. Key Features

- **Jetson Orin NX SoM integration:** powered by the NVIDIA Jetson Orin NX SoM, which includes a high-performance GPU, AI accelerators, and a multi-core ARM CPU, optimized for power-efficient edge AI workloads.
- **PXIe form factor:** modular design that fits into the PXIe chassis, providing an ideal solution for scalable edge AI systems and easy integration into larger test and measurement environments.
- **Add-on board connector:** supports the addition of add-on boards, enabling the integration of specialized features like GMSL2 and 3G-SDI interfaces. These high-bandwidth interfaces are routed from the Jetson platform via the add-on boards, allowing for flexible customization.
- **Edge AI optimization:** designed to run AI algorithms locally at the edge, minimizing data transfer to the cloud and reducing latency for faster, real-time processing.
- **Customizable and scalable:** the modular design allows users to expand the platform with custom add-on boards to meet specific project requirements and ensure scalability for a wide range of applications.

2. Hardware Overview

2.1. Circuitry

The PXIe Jetson Orin NX Module integrates the NVIDIA Jetson Orin NX SoM, which includes a high-performance GPU (Ampere architecture), deep learning accelerators (NVIDIA Tensor Cores), and a multi-core ARM CPU. The system is designed to run intensive AI models directly at the edge, ensuring real-time processing. Additionally, the module supports modular I/O expansion via the add-on board connector, enabling custom hardware additions such as GMSL2 and 3G-SDI for high-speed data transfer.

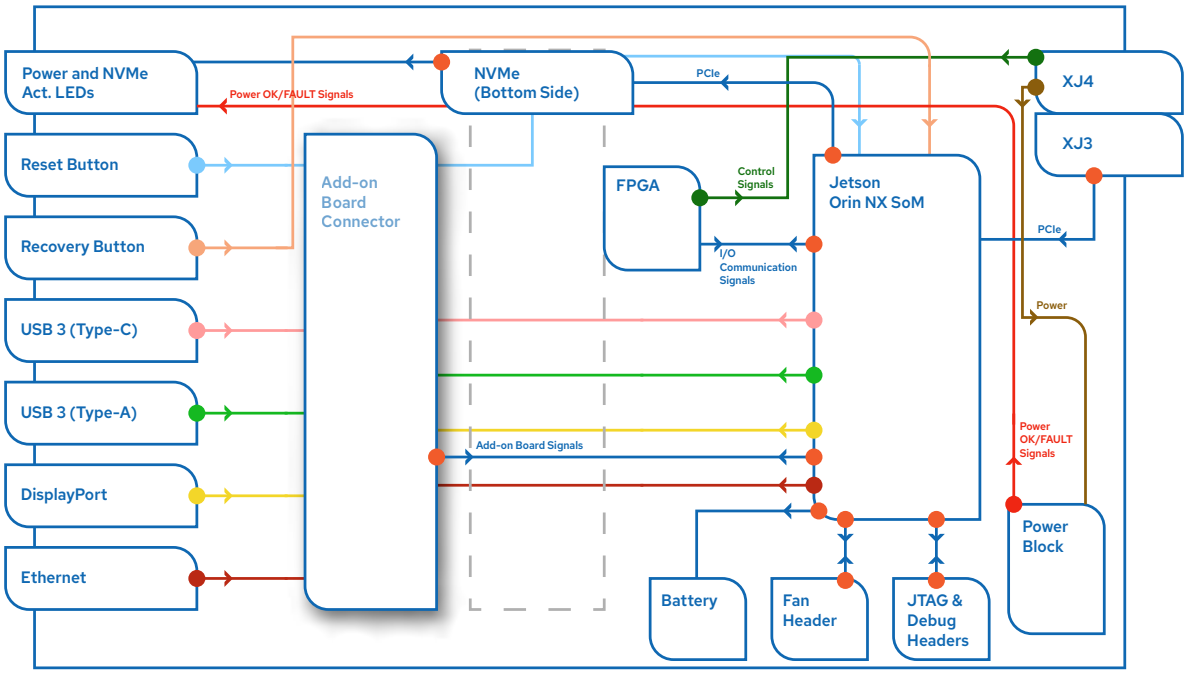

Figure 1: Block Diagram of the Carrier Board

2.2. Hardware Specifications

- **Processor:** NVIDIA Jetson Orin NX SoM with Ampere GPU, 8-core ARM Cortex-A78AE v8.2 64-bit CPU, and tensor cores
- **Memory:** 16 GB LPDDR5, 102.4 GB/s memory bandwidth
- **Storage:** supports NVMe (via M.2) for external storage
- **PXIe interface:** 4-lane PCIe Gen4 (ctrl #4) for high-speed data communication
- **Video outputs:** supports DisplayPort (via dedicated connector or add-on boards) and various high-performance visual outputs via add-on boards
- **I/O connectivity:** USB type-C, USB type-A, gigabit ethernet, DisplayPort, and additional options via add-on board connector

2.2.1. USB Ports

The carrier board supports 2 USB connectors. One is a USB 3.2 type-C connector (J7) supporting host, device, and USB recovery. In addition, there is a 3.2 type-A connector (J6) that supports host mode only.

Table 1: USB 3.2 Type-C Connector Pin Description – J7

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description
A1	–	–	Ground
A2	USBSS1_TX_P	47	USB 3.2 #1 transmit 1 from mux
A3	USBSS1_TX_N	45	
A4	–	–	USB VBUS power
A5	–	–	CC 1 from CC controller
A6	USB0_D_P	111	USB 2.0 #0 Data 1
A7	USB0_D_N	109	
A8	–	–	Unconnected
A9	–	–	USB VBUS power
A10	USBSS1_RX_P	39	USB 3.2 #1 receive 2 from mux
A11	USBSS1_RX_N	41	
A12	–	–	Ground
B1	–	–	Ground
B2	USBSS1_TX_P	47	USB 3.2 #1 transmit 2 from mux
B3	USBSS1_TX_N	45	
B4	–	–	USB VBUS power
B5	–	–	CC 2 from CC controller
B6	USB0_D_P	111	USB 2.0 #0 data 2
B7	USB0_D_N	109	
B8	–	–	Unconnected
B9	–	–	USB VBUS power
B10	USBSS1_RX_P	39	USB 3.2 #1 receive 1 from mux
B11	USBSS1_RX_N	41	
B12	–	–	Ground

Table 2: USB 3.2 Type-A Connector Pin Description – J6

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description
1	–	–	VBUS supply
2	USB1_D_N	115	USB 2.0 #1 data
3	USB1_D_P	117	
4	–	–	Ground
5	USBSS0_RX_N	161	USB 3.2 #0 receive
6	USBSS0_RX_P	163	
7	–	–	Ground
8	USBSS0_TX_N	166	USB 3.2 #0 transmit
9	USBSS0_TX_P	168	

2.2.2. Gigabit Ethernet

The carrier board implements an RJ45 connector (J4) along with the necessary magnetics device.

Table 3: Ethernet RJ45 Connector Pin Description – J4

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description
1	–	–	MCT
2	GBE_MDI0_P	186	Gigabit ethernet MDI 0+
3	GBE_MDI0_N	184	Gigabit ethernet MDI 0-
4	GBE_MDI1_P	192	Gigabit ethernet MDI 1+
5	GBE_MDI1_N	190	Gigabit ethernet MDI 1-
6	GBE_MDI2_P	198	Gigabit ethernet MDI 2+
7	GBE_MDI2_N	196	Gigabit ethernet MDI 2-
8	GBE_MDI3_P	204	Gigabit ethernet MDI 3+
9	GBE_MDI3_N	202	Gigabit ethernet MDI 3-
10	–	–	CHASSIS
11	–	–	Green LED anode
12	GBE_LED_LINK	188	Green LED cathode. On for 1000 Mb/s link. Off for 10/100 Mb/s.
13	GBE_LED_ACT	194	Yellow LED cathode. On indicates activity
14	–	–	Yellow LED anode

2.2.3. DisplayPort

The module is equipped with a DisplayPort channel, which is routed through a hardware-configurable switch. This provides flexible options to direct the video signal to the front-panel DisplayPort connector (J5) or the add-on board connector, depending on the specific use case.

Configuration options for DisplayPort (SW1301):

- Via dedicated DisplayPort connector (SW: Off)
- Via add-on board connector for additional custom interfaces and configurations (SW: On)

Table 4: DisplayPort Connector Pin Description – J5

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description
1	DP0_TXD0_P	41	DP lane 0+
2	–	–	Ground
3	DP0_TXD0_N	39	DP lane 0-
4	DP0_TXD1_P	47	DP lane 1+
5	–	–	Ground
6	DP0_TXD1_N	45	DP lane 1-
7	DP0_TXD2_P	53	DP lane 2+
8	–	–	Ground
9	DP0_TXD2_N	51	DP lane 2-
10	DP0_TXD3_P	59	DP lane 3+
11	–	–	Ground
12	DP0_TXD3_N	57	DP lane 3-
13	–	–	MODE to support dual-role mode. Connects from DP connector to PI3AUX221ZTAEX device to select between DP or HDMI modes
14	–	–	CEC_DP: not used – pulled to GND through 1 Mohm resistor
15	DP0_AUX_N	90	DisplayPort auxiliary channel 0-
16	–	–	Ground
17	DP0_AUX_P	92	DisplayPort auxiliary channel 0+
18	DP0_HPD	88	HDMI hot plug detect
19	–	–	Power return (ground)
20	–	–	+3.3 V

2.2.4. M2 Key M Expansion Slot

The carrier board includes a M.2, Key M Slot for NVMe storage (J3). The M.2, Key M slot supports PCIe (x1), Gen4.

Table 5: M.2 Key M Expansion Slot Pin Description – J3

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description	Pin #	Associated Module Pin Name	Module Pin #	Usage/Description
1 3	–	–	Ground	2 4	–	–	Main 3.3 V supply
5 7	–	–	Unused	6 8	–	–	Unused
9	–	–	Ground	10	–	–	NVMe drive (LED)
11 13	–	–	Unused	12 14 16 18	–	–	Main 3.3 V supply
15	–	–	Ground				
17 19	–	–	Unused				
21	–	–	Ground	20 22 24 26 28 30 32 34 36 38 40 42	–	–	Unused
23 25	–	–	Unused				
27	–	–	Ground				
29 31	–	–	Unused				
33	–	–	Ground				
35 37	–	–	Unused				
39	–	–	Ground				
41	PCIE1_RX0_N	167	PCIe ctrl #1 lane 0 receive				
43	PCIE1_RX0_P	169		44	GPIO10	212	M.2 key M alert
45	–	–	Ground	46 48	–	–	Unused
47	PCIE1_TX0_N	172	PCIe ctrl #1 lane 0 transmit				
49	PCIE1_TX0_P	174		50	PCIE1_RST*	183	PCIe ctrl #1 reset
51	–	–	Ground	52	PCIE1_CLKREQ*	182	PCIe ctrl #1 clock request
53	PCIE1_CLK_N	173	PCIe ctrl #1 reference clock	54	PCIE_WAKE*	179	
55	PCIE1_CLK_P	175		56 58	–	–	Unused
57	–	–	Ground				
67 69	–	–	Unused	68	–	–	32 kHz suspend clock
71 73 75	–	–	Ground	70 72 74	–	–	Main 3.3 V supply

2.2.5. PXIe Interface

The module utilizes a high-bandwidth 4-lane PCIe Gen4 interface (ctrl #4) to ensure rapid data communication between the Jetson Orin NX platform and the PXIe backplane. This high-speed link provides the necessary throughput for data-intensive AI workloads, seamless sensor integration, and real-time processing within the PXIe ecosystem.

Table 6: PXIe Connector Pin Description – XJ4

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description	Pin #	Associated Module Pin Name	Module Pin #	Usage/Description
A1	–	–	PXIe 100 MHz clock	**B1**	-	-	PXIe 100 MHz clock
A2	–	–	Unused	**B2**	-	-	Unused
A3	–	–	PXIe SMBus	**B3**	-	-	PXIe SMBus
A4	–	–	Unused	**B4**	PCIE0_RST*	181	PCIe ctrl #4 reset
A5	PCIE0_TX0_P	136	PCIe ctrl #4 lane 0	**B5**	PCIE0_TX0_N	134	PCIe ctrl #4 lane 0
A6	PCIE0_TX2_P	150	PCIe ctrl #4 lane 2	**B6**	PCIE0_TX2_N	148	PCIe ctrl #4 lane 2
A7	PCIE0_TX3_P	156	PCIe ctrl #4 lane 3	**B7**	PCIE0_TX3_N	154	PCIe ctrl #4 lane 3
A8	–	–	Unused	**B8**	–	–	Unused
A9	–	–	Unused	**B9**	–	–	Unused
A10	–	–	Unused	**B10**	–	–	Unused
C1	–	–	PXIe SYNC100 signal	**D1**	–	–	PXIe SYNC100 signal
C2	–	–	PXIe DSTARB signal	**D2**	–	–	PXIe DSTARB signal
C3	–	–	Unused	**D3**	–	–	Unused
C4	–	–	Unused	**D4**	–	–	Unused
C5	PCIE0_RX0_P	133	PCIe ctrl #4 lane 0	**D5**	PCIE0_RX0_N	131	PCIe ctrl #4 lane 0
C6	PCIE0_RX2_P	151	PCIe ctrl #4 lane 2	**D6**	PCIE0_RX2_N	149	PCIe ctrl #4 lane 2
C7	PCIE0_RX3_P	157	PCIe ctrl #4 lane 3	**D7**	PCIE0_RX3_N	155	PCIe ctrl #4 lane 3
C8	–	–	Unused	**D8**	–	–	Unused
C9	–	–	Unused	**D9**	–	–	Unused
C10	–	–	Unused	**D10**	–	–	Unused
E1	–	–	PXIe DSTARC signal	**F1**	–	–	PXIe DSTARC signal
E2	–	–	PXIe DSTARA signal	**F2**	–	–	PXIe DSTARA signal
E3	–	–	Unused	**F3**	–	–	Unused
E4	PCIE0_CLK_P	162	PCIe ctrl #4 reference clock	**F4**	PCIE0_CLK_N	160	PCIe ctrl #4 reference clock
E5	PCIE0_TX1_P	142	PCIe ctrl #4 lane 1	**F5**	PCIE0_TX1_N	140	PCIe Ctrl #4 lane 1
E6	PCIE0_RX1_P	139	PCIe ctrl #4 lane 1	**F6**	PCIE0_RX1_N	137	PCIe Ctrl #4 lane 1
E7	–	–	Unused	**F7**	–	–	Unused
E8	–	–	Unused	**F8**	–	–	Unused
E9	–	–	Unused	**F9**	–	–	Unused
E10	–	–	Unused	**F10**	–	–	Unused

2.2.6. Add-on Board Connector

The carrier board includes a 240-pin add-on board connector. The connector used on the carrier board is a SAMTEC (part # SEAM-40-11.0-S-06-2-A-K-TR). The add-on board connector includes various interfaces including:

- Two 4-lane or four 2-lane MIPI D-PHY CSI
- 2-lane PCIe (Ctrl #7)
- Three I2C (CAM, I2C0, I2C1)
- One SPI (SPI1)
- One UART (UART0)
- One I2S (I2S1)
- One CAN
- One DisplayPort through a hardware configurable switch (SW1301)

Table 7: Add-on Board Connector – J2

Pin	A	B	C	D	E	F
1	CSI1_D1_P	GND	CSI3_D1_P	GND		GND
2	CSI1_D1_N	GND	CSI3_D1_N	GND		GND
3	GND	CSI1_D0_P	GND	CSI3_D0_P	GND	
4	GND	CSI1_D0_N	GND	CSI3_D0_N	GND	
5	CSI1_CLK_P	GND	CSI3_CLK_P	GND		GND
6	CSI1_CLK_N	GND	CSI3_CLK_N	GND		GND
7	GND	CSI0_D1_P	GND	CSI2_D1_P	GND	
8	GND	CSI0_D1_N	GND	CSI2_D1_N	GND	
9	CSI0_D0_P	GND	CSI2_D0_P	GND		GND
10	CSI0_D0_N	GND	CSI2_D0_N	GND		GND
11	GND	CSI0_CLK_P	GND	CSI2_CLK_P	GND	DP1_AUX_CH_EXT_P
12	GND	CSI0_CLK_N	GND	CSI2_CLK_N	GND	DP1_AUX_CH_EXT_N
13		GND		GND	DP1_TX3_EXT_P	GND
14		GND		GND	DP1_TX3_EXT_N	GND
15	GND		GND		GND	DP1_TX2_EXT_P
16	GND		GND		GND	DP1_TX2_EXT_N

Pin	A	B	C	D	E	F
17		GND		GND	DP1_TX1_EXT_P	GND
18		GND		GND	DP1_TX1_EXT_N	GND
19	GND		GND		GND	DP1_TX0_EXT_P
20	GND		GND		GND	DP1_TX0_EXT_N
21		GND		GND		GND
22		GND		GND	DP1_HPD_LS_EXT	HDMI_CEC_EXT
23	GND		GND		GND	PCIE2_CLKREQ*
24	GND		GND		GND	PCIE2_RST*
25	CAM0_MCLK	GND	MCLK2/GPIO01	GND	PCIE2_TX0_N	GND
26	CAM_I2C_SDA	GND	CAM1_RST/ GPIO03	GND	PCIE2_TX0_P	GND
27	CAM_I2C_SCL	CAM1_MCLK	CAM1_PWDN	MCLK3/GPIO11	GND	PCIE2_RX0_N
28	I2C0_SDA	CAM0_RST/ GPIO02	AVDD_ CAM_2V8_ ENABLE/ GPIO05	FPGA_AB_PS_ RST	GND	PCIE2_RX0_P
29	I2C0_SCL	CAM0_PWDN	VDD_SYS_ ENABLE/ GPIO06	GND	PCIE2_TX1_N	GND
30	I2C1_SDA	GND		GND	PCIE2_TX1_P	GND
31	I2C1_SCL	AUD_MCLK/ GPIO09		FPGA_AB_PS_ UART1_RX	GND	PCIE2_RX1_N
32	GND	I2S1_DIN	GND	FPGA_AB_PS_ UART1_TX	GND	PCIE2_RX1_P
33	UART0_CTS*	I2S1_FS	CAN_RX	GND	PCIE2_CLK_N	GND
34	UART0_RXD	I2S1_DOUT	CAN_TX	GND	PCIE2_CLK_P	GND
35	UART0_TXD	AUD_CODEC_ INT/GPIO07	SPI1_CS1*	FPGA_AB_TDO	GND	PCIE_WAKE*
36	UART0_RTS*	I2S1_SCLK	SPI1_CS0*	FPGA_AB_TDI	FPGA_AB_ PROGRAM_B	GND
37	GND	SPI1_SCK	SPI1_MISO	FPGA_AB_TMS	GND	VCC_5V0
38	VDD_3V3	GND	SPI1_MOSI	FPGA_AB_TCK	GND	VCC_5V0
39	VDD_3V3	GND	GND	GND	GND	VCC_5V0
40	VDD_3V3	GND	VDD_1V8	VDD_1V8	GND	VCC_5V0

2.2.7. Debug and JTAG Headers

The carrier board is equipped with two 30-pin headers (J8 and J9) designed for system-level monitoring, debugging, and FPGA programming. These connectors provide external access to critical system signals, dedicated UART debug interfaces, and JTAG ports.

- **System signals header (J8):** this header provides access to system control signals (such as reset and recovery), and a dedicated UART interface for serial debugging of the module.
- **FPGA JTAG and debug header (J9):** this connector is primarily used for JTAG access to both the carrier board FPGA and the add-on board (AB) FPGA. It also includes FPGA configuration and status signals to facilitate hardware-level troubleshooting and programming.

Table 8: System Signals Header – J8

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description	Pin #	Associated Module Pin Name	Module Pin #	Usage/ Description
1	–	–	1.8 V	2	–	–	Ground
3	–	–	Unused	4	–	–	Ground
5	–	–	Unused	6	–	–	Ground
7	–	–	Unused	8	–	–	Ground
9	–	–	Unused	10	–	–	Ground
11	–	–	Unused	12	–	–	Ground
13	SYS_RESET*	239	System reset	14	–	–	Ground
15	FORCE_RECOVERY*	214	Force recovery mode	16	–	–	Ground
17	SLEEP/WAKE*	240	Initiate power-on if Auto-PowerOn disabled	18	–	–	Ground
19	MOD_SLEEP*	178	Module sleep	20	–	–	Ground
21	UART2_RXD	238	UART #2 (Debug)	22	–	–	Ground
23	UART2_TXD	236	UART #2 (Debug)	24	–	–	Ground
25	–	–	Unused	26	–	–	Ground
27	–	–	Unused	28	–	–	Ground
29	–	–	3.3 V	30	–	–	Ground

Table 9: FPGA JTAG and Debug Signals Header – J9

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description	Pin #	Associated Module Pin Name	Module Pin #	Usage/Description
1	–	–	3.3 V	2	–	–	1.8 V
3	–	–	Ground	4	–	–	Ground
5	–	–	FPGA TDO (AB)	6	–	–	FPGA PS reset (AB)
7	–	–	FPGA TDI (AB)	8	–	–	FPGA Program_B (AB)
9	–	–	FPGA TMS (AB)	10	–	–	FPGA PS UART RX (AB)
11	–	–	FPGA TCK (AB)	12	–	–	FPGA PS UART TX (AB)
13	–	–	Ground	14	–	–	Ground
15	–	–	Ground	16	–	–	Ground
17	–	–	Ground	18	–	–	Ground
19	–	–	FPGA TDO	20	–	–	Unused

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description	Pin #	Associated Module Pin Name	Module Pin #	Usage/Description
21	–	–	FPGA TDI	22	–	–	FPGA Program_B
23	–	–	FPGA TMS	24	–	–	FPGA UART RX
25	–	–	FPGA TCK	26	–	–	FPGA UART TX
27	–	–	Ground	28	–	–	Ground
29	–	–	3.3 V (FPGA)	30	–	–	Ground

2.2.8. Fan Connector

The carrier board includes a 4-pin fan header (J13). The connector used is a Molex (Part # 0470531000).

Table 10: Fan Connector Pin Description – J10

Pin #	Associated Module Pin Name	Module Pin #	Usage/Description
1	–	–	Ground
2	–	–	Main 5.0 V supply
3	GPIO08	208	Fan tachometer signal
4	GPIO14	230	Fan pulse width modulation signal

2.2.9. Electrical Specifications

The simple power diagram of the DE160202 module is given in Figure 2.

Note

DE160202 module has pull-up on MODULE_ID. So, both 5 V and HV mode supported.

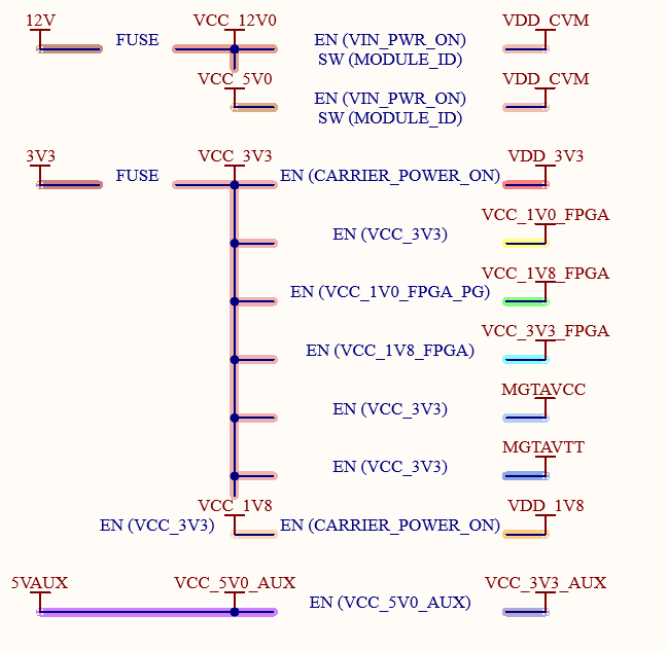

Figure 2: Power Diagram

The power supply requirements of the DE160202 module are given in Table 11.

Table 11: Power Supply Requirements

Specification	Min	Typical	Max	Units
Power Supply Current of 12 V (XJ4)	–	–	5.5	A
Power Supply Current of 3.3 V (XJ4)	–	–	7	A
Power supply current of 5 VAUX (XJ4)	–	–	0.1	A

2.2.10. Physical Specifications

DE160202 is compatible with the two-slot 3U PXIe peripheral module slots in the PXIe chassis.

2.2.11. Environmental Specifications

The environmental specifications of the module are given in Table 12.

Table 12: Environmental Specifications

Specification	Condition	Value
Operating Humidity	Relative, non-condensing	10% - 90%
Storage Humidity	Relative, non-condensing	5% - 95%
Operating Temperature	Forced-air cooling from chassis	0°C - +40°C
Storage Temperature	–	-40°C - +85°C

3. Software Overview

This device is PXI Express compatible.

4. Safety Guidelines

Caution

The DE160202 shall not be operated in any manner not specified in this document. Misuse of the product may result in a hazard. Safety protection features may be compromised if the product is damaged. In the event of damage, the product shall be returned for repair.

6. Compatibility Guidelines

This product has been tested and found to comply with the applicable regulatory requirements and limits for electromagnetic compatibility (EMC). These requirements and limits are intended to provide reasonable protection against harmful interference when the product is operated within the specified electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in certain installations if the product is connected to peripheral devices or test objects, or if it is used in residential or commercial areas. To minimize interference with radio and television reception and to prevent unacceptable performance degradation, the product shall be installed and operated in strict accordance with the instructions specified in the product documentation.

Any changes or modifications to the product not expressly approved by DEICO may void the user's authority to operate the equipment under local regulatory rules.

Caution

To ensure the specified EMC performance, the product shall be operated only with shielded cables and accessories.

Caution

To ensure the specified EMC performance, the length of any cable attached to the front connectors shall not exceed 3 m (10 ft.).

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