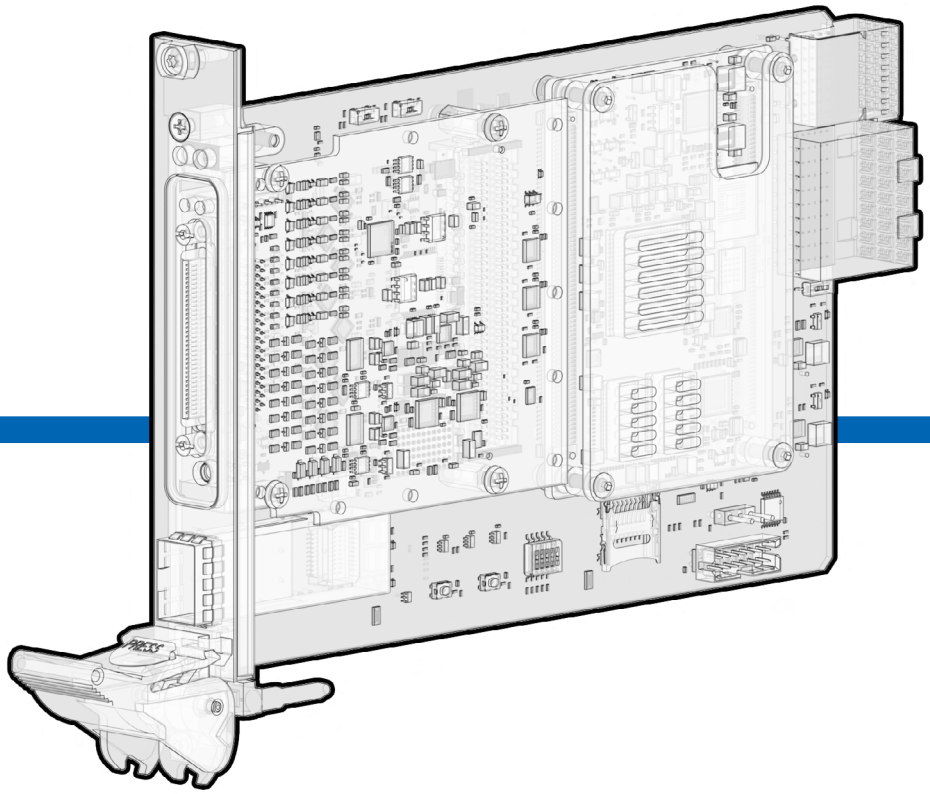
Datasheet



DE140900

PXIe Digital Analog I/O Module

DEICO

www.deico.com.tr

Contents

1. Description

DE140900 PXIe Digital Analog I/O Module is a fully integrated digital and analog I/O system. This system provides 16 digital I/O, 16 single-ended or 8 differential analog inputs, and 8 analog output channels. All I/O channels are routed to the front panel VHDCI connectors. The module includes a flexible digital I/O system that can interface with multiple logic families and all digital channels feature a programmable threshold level.

The DE140900 features an 18-bit, simultaneous sampling, analog-to-digital Data Acquisition (DAQ) system that is configurable for 16 single-ended or 8 differential channels. Each input channel is equipped with analog clamp protection.

The module also provides an 8-channel, 16-bit analog output stage with a precision reference. Each output is independently programmable to a range of ±15 V. The analog outputs are guaranteed monotonic and include built-in rail-to-rail buffers capable of sourcing or sinking up to 55 mA. These outputs can be automatically calibrated using the integrated ADC block.

1.1. Key Features

- Flexible and expandable PXIe module
- Full size ruggedized LPC FMC module
- Fully protected analog and digital I/O
- MTBF > 150,000 hours
- Lines protected up to 7 kV electrostatic discharge
- PC-based or standalone/embedded controller operation
- Supported by PXIe Chassis

Standards and Compliance

- Environmental: IEC 60068-2-1, IEC 60068-2-2, IEC 60068-2-27, IEC 60068-2-64, IEC 60068-2-78
- EMC/EMI: EN 61326, EN 55011 (CISPR 11), AS/NZS CISPR 11, FCC 47 CFR Part 15B, ICES-001

Typical Applications

- High-density measurement and sensing
- Data Acquisition (DAQ) systems
- Instrumentation and control systems
- Automated Test Equipment (ATE)
- Process control and industrial automation
- Hardware-in-the-Loop (HIL) simulation

1.2. Analog Input

Features an 18-bit, simultaneous-sampling, Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC).

Channel Configuration

- 16 single-ended channels
- 8 differential channels

Performance

- Sampling rate: 1 MS/s (megasample per second)
- Selectable bandwidth: 2 kHz and 220 kHz (per channel)

Input Ranges (per-channel selectable)

- Bipolar single-ended: ±12.5 V, ±10 V, ±6.25 V, ±5 V, ±2.5 V
- Unipolar single-ended: 0 V to 12.5 V, 0 V to 10 V, 0 V to 5 V
- Bipolar differential: ±15 V, ±12.5 V, ±10 V, ±5 V

Input Protection

- Input impedance: 1.2 MΩ
- ESD protection: ±6 kV
- Input clamp protection: ±21 V (up to ±48 V)

1.3. Analog Output

Features an 8-channel, 16-bit, Digital-to-Analog Converter (DAC) with an integrated precision reference.

Output Stage

- Guaranteed monotonic performance
- Integrated rail-to-rail output buffers
- Current drive: ±55 mA (source/sink)

Output Ranges (independently programmable per channel)

- Unipolar: 0 V to 5 V, 0 V to 10 V
- Bipolar: ±5 V, ±10 V, ±15 V

Performance and Accuracy

- Settling time: <15 µs
- Integral Non-Linearity (INL): ±3 LSB (max)
- Calibration: all channels feature automatic calibration using the internal ADC

1.4. Digital Input/Output

Features a high-speed, flexible digital I/O system designed for hardware-timed control and digital device testing.

Performance

- Data rate: up to 420 Mb/s
- Timing: precision hardware-timed control

Architecture

- Provides 2 bidirectional digital channels, with each channel consisting of 8 bit (16 bit total).
- Each channel's direction (input or output) is independently configurable.

Programmable Logic Levels

- The core feature is the programmable voltage thresholds, adjustable from 1.1 V to 5.25 V.
- This allows the module to directly interface with various logic families (e.g., TTL, CMOS, LVCMOS) without external level-shifting circuitry.
- Enables precise characterization of a Device Under Test's (DUT) input voltage thresholds (V_{IL}, V_{IH}), as illustrated in Figure 1.

Input/Output Characteristics

- Input buffers: all inputs feature Schmitt-trigger buffers for high noise immunity and reliable operation with slow-slewing or noisy signals
- Supported states: supports logic low (0), logic high (1), and high-impedance (Tri-state, Z) for advanced waveform generation and bus simulation
- Output Drive Capacity: 32 mA per channel
- Current Clamping: ±50 mA per channel

The programmable input (V_{IH}, V_{IL}) and output (V_{OH}, V_{OL}) voltage levels allow the DE140900 to interface directly with a wide range of devices.

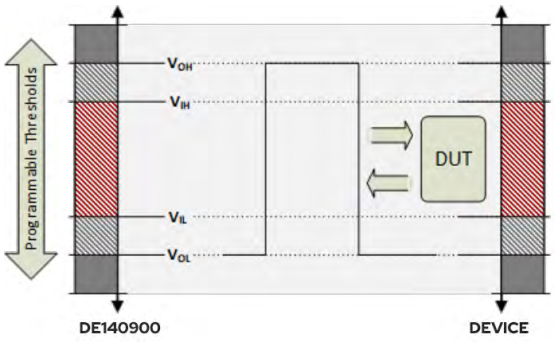


Figure 1: Flexible Digital I/O Interface with Programmable Thresholds

1.5. External Trigger Input

The FMC module features a high-speed trigger input utilizing a low-jitter repeater. This stage converts single-ended signals to differential LVDS with a very low propagation delay of 1 ns and a typical RMS jitter of 1.2 ps, ensuring precise timing synchronization for high-speed FPGA applications.

2. Hardware Overview

2.1. Functional Block Diagram

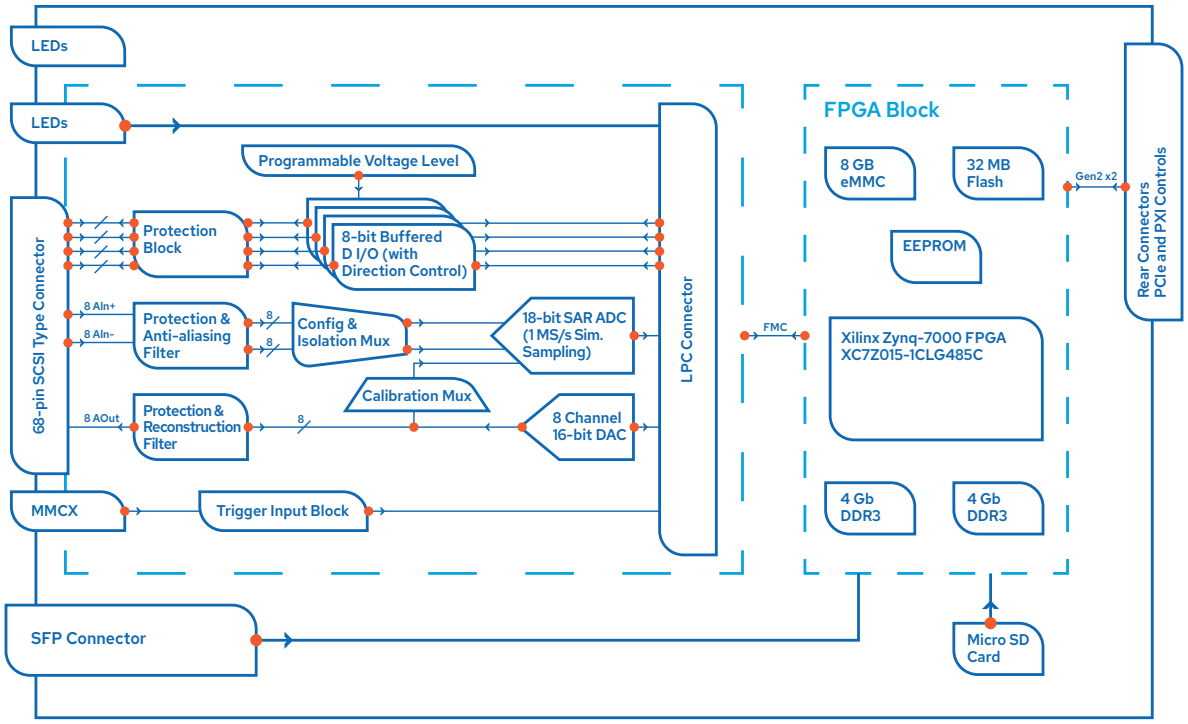


Figure 2: Block Diagram of DE140900 PXIe Digital Analog I/O Module

2.2. Hardware Specifications

2.2.1. Electrical Specifications

Table 1: Electrical Specifications

Specification	Description
Input Voltage	+12 V, +5 VAUX, +3.3 V DC (from backplane)
Power Consumption	Typical: 4 W Maximum: 13 W

Table 2: Analog Inputs

Specification	Description
Number of Channels	16 single-ended or 8 fully differential (software-selectable)
ADC Resolution/Architecture	18 bit / SAR (Successive Approximation Register)
Sampling Rate	1 MS/s (megasample per second)
Simultaneous Sampling	Differential: 8 channels Single-ended: 8 channels
Bandwidth	Selectable: 2 kHz and 220 kHz (per channel)
INL (Integral Non-Linearity)	±4 LSB (max)
DNL (Differential Non-Linearity)	±2 LSB (max)
Offset / Gain Error Drift	±0.5 ppm/°C (typical)
Input Ranges (per channel)	Bipolar single-ended: ±12.5 V, ±10 V, ±6.25 V, ±5 V, ±2.5 V Unipolar single-ended: 0 V to 12.5 V, 0 V to 10 V, 0 V to 5 V Bipolar differential: ±15 V, ±12.5 V, ±10 V, ±5 V
Input Impedance	1.2 MΩ
Protection	Input clamp: ±21 V (up to ±48 V) ESD (human body model): ±6 kV
Input Channel Control	Each channel can be programmatically disconnected (set to a high impedance state) from the ADC input.

Table 3: Analog Outputs

Specification	Description
Number of Channels	8
Resolution	Full 16-bit resolution at all ranges
Voltage Output Ranges	0 V to 5 V, 0 V to 10 V, ±5 V, ±10 V, ±15 V (independently programmable output ranges)
Output Impedance	0.01 Ω
DAC Type	Voltage - Buffered
INL Error	±3 LSB (max)
Outputs Drive Current	±55 mA (guaranteed)
Settling Time	<15 µs (to ±1 LSB at 16 bits)
Capacitive Load Driving	1000 pF
Voltage Output Slew Rate	>3.5 V/µs
Output Current Limit	±115 mA
Gain Temperature Coefficient	2 ppm/°C
Protection	Resettable PTC fuse and ESD protection

Table 4: Digital I/O

Specification	Description
Threshold Voltage Accuracy	±10 mV (over 0 V to 5.25 V DC)
Total Number of Bits	16 (2 channel x 8 bit)
Number of Channels	2
Width per Channel	8 bits
Direction Control	Per-channel, independently configurable
Maximum Data Rate	420 Mb/s
Drive Capacity (per channel)	±32 mA (continuous)
Input Voltage Thresholds	Programmable, 0 V to 5.25 V
Output Voltage Levels	Programmable, 1.1 V to 5.25 V (supports open-drain configuration)
ESD Protection	±7 kV (human body model)
Current Clamping	±50 mA
Output Type	Tri-state, non-inverted
Input Type	Schmitt-trigger inputs allow for slow or noisy inputs

Table 5: Trigger Input

Specification	Description
Input Interface	MMCX
Input Impedance(Z_{IN})	50 Ω
Operating Input Voltage(V_{IH}) / (V_{IL})	1.65 V / 5.0 V
Continuous Overload(V_{MAX})	±7.5 V
Transient Overload (V_{TR})	±10 V
Max Data Rate	400 Mb/s
Propagation Delay (t_{PD})	1 ns
RMS Jitter ($t_{JIT(RMS)}$)	1.2 ps
Part-to-Part Skew	500 ps

2.2.2. Physical Specifications

Table 4: Physical Specifications

Specification	Description
Dimensions (L / W)	200 mm x 130.5 mm (3U rack height)
Height (H)	4 HP (20.32 mm)
Front Panel Connectors (x2)	68-pin VHDCI connector

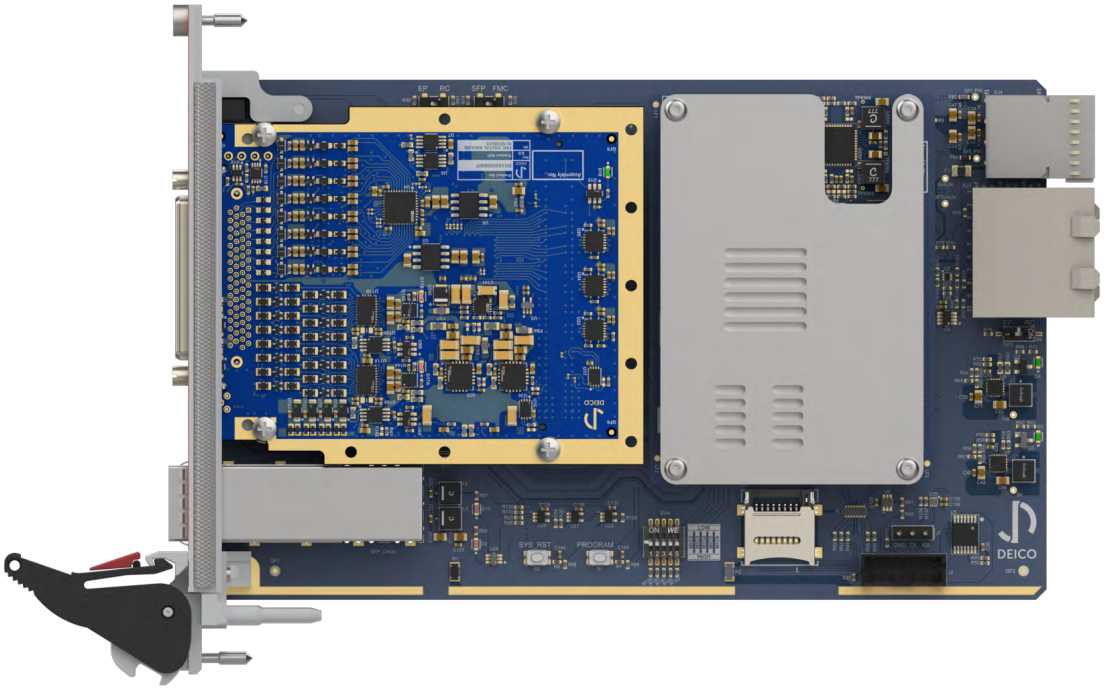


Figure 3: DE140900 PXIe Digital Analog I/O Module

2.2.3. Environmental Specifications

Table 3: Environmental Specifications

Specification	Condition	Value
Operating Humidity	Relative, non-condensing	10% - 90%
Storage Humidity	Relative, non-condensing	5% - 95%
Operating Temperature	Forced-air cooling from chassis	0 °C - +40 °C
Storage Temperature	–	-40 °C – +85 °C

3. Software Overview

This module is compatible with IVISwtch class.

4. Signal Connections

4.1. I/O Connector

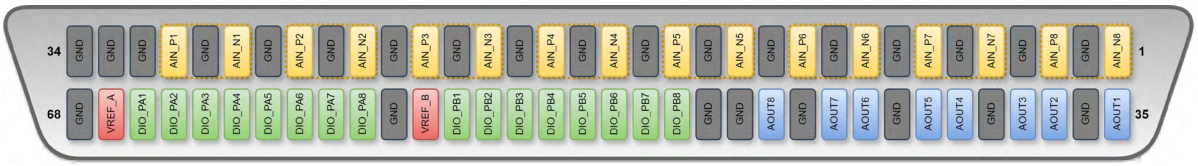


Figure 4: DB68 Pinout Diagram

5. Safety Guidelines

Caution

The DE140900 shall not be operated in any manner not specified in this document. Misuse of the product may result in a hazard. Safety protection features may be compromised if the product is damaged. In the event of damage, the product shall be returned for repair.

6. Compatibility Guidelines

This product has been tested and found to comply with the applicable regulatory requirements and limits for electromagnetic compatibility (EMC). These requirements and limits are intended to provide reasonable protection against harmful interference when the product is operated within the specified electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in certain installations if the product is connected to peripheral devices or test objects, or if it is used in residential or commercial areas. To minimize interference with radio and television reception and to prevent unacceptable performance degradation, the product shall be installed and operated in strict accordance with the instructions specified in the product documentation.

Any changes or modifications to the product not expressly approved by DEICO may void the user's authority to operate the equipment under local regulatory rules.

Caution

To ensure the specified EMC performance, the product shall be operated only with shielded cables and accessories.

Caution

To ensure the specified EMC performance, the length of any cable attached to the front connectors shall not exceed 3 m (10 ft.).

support@**deico.com.tr**
+90 312 395 68 44