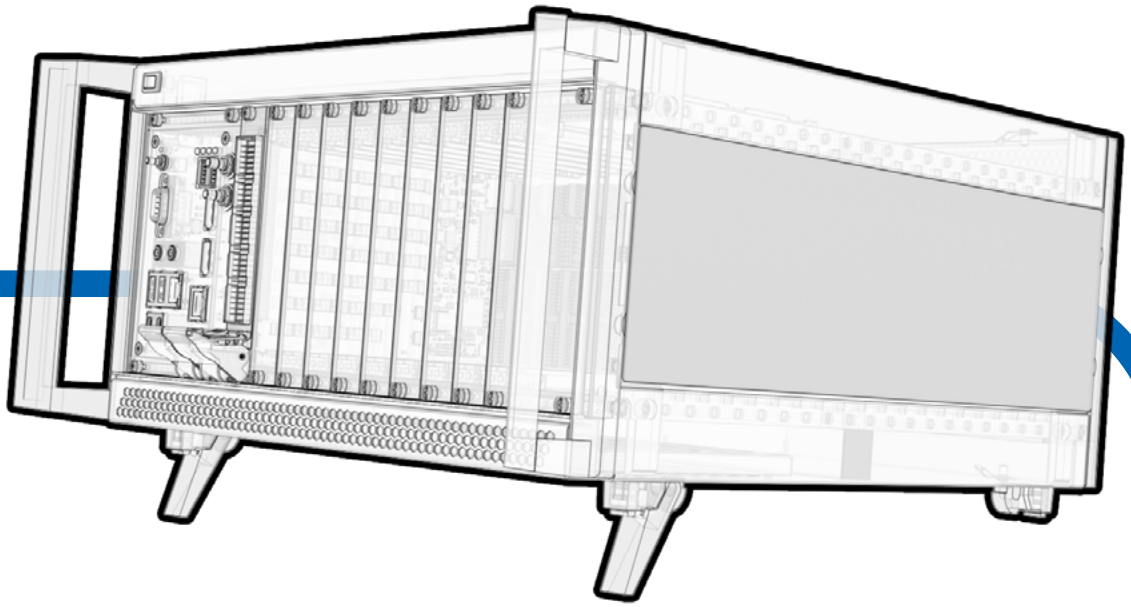
Datasheet



DE140000

PXIe Chassis

10 Slot 4 Link Gen 3

DEICO

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1. Description

PXIe Chassis 10 Slot 4 Link Gen 3 is a 10 slot PXIe chassis. This device creates a test environment by connecting system modules and peripheral modules with PCIe protocol.

1.1. Key Features

- 1 system slot, 9 hybrid peripheral slots
- 4-link configuration (4 x 4)
- PCI Express Gen 3 x 4
- 16 GB/s system bandwidth
- 32-bit, 33/66 MHz PCI legacy support
- Inhibit mode and fan mode selection
- 4 PFI interfaces
- External reference clock input / output
- SMBus support
- Total 1000 W power capability
- 82 W slot cooling capability

DE140000 is compatible with IEC 60068-2-1 / IEC 60068-2-2 / IEC 60068-2-78 / IEC 60068-2-27 / IEC 60068-2-64 / EN 61326 (IEC 61326) / EN 55011 (CISPR 11) / AS / NZS CISPR 11 / FCC 47 CFR Part 15B / ICES-001 standarts.

Areas of application include:

- LAB usage
- Modular test systems
- Automated test equipment

2. Hardware Overview

2.1. Functional Block Diagram

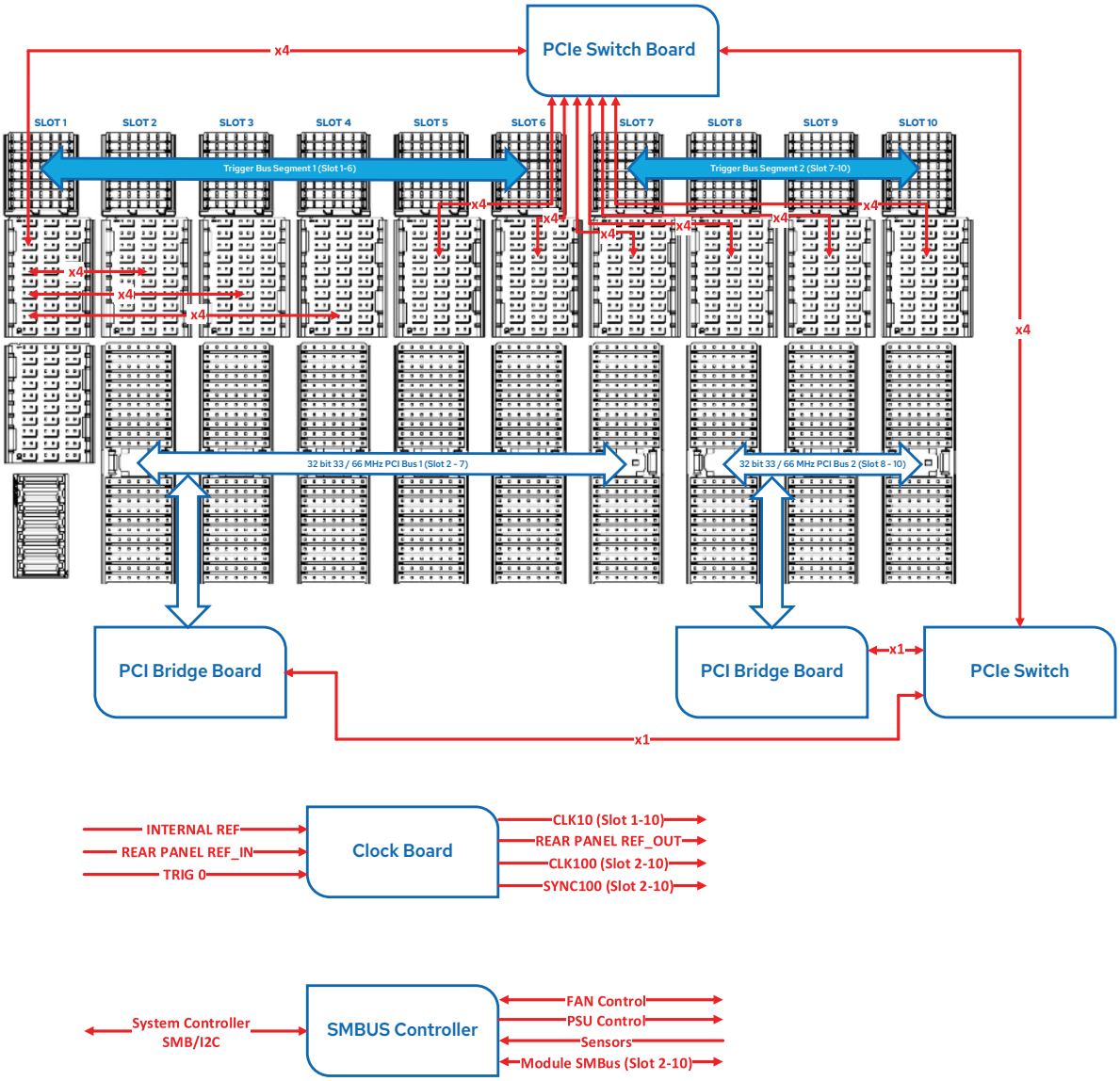

Figure 1: DE140000 Chassis PCIe Connection Diagram

2.2. Hardware Specifications

2.2.1. Electrical

Table 1: Electrical Specifications

Specification	Min	Typ	Max	Notes
Input Voltage	100 V AC	220 V AC	240 V AC	-
Input Voltage Frequency	47 Hz	50 Hz	63 Hz	-
Input Current	-	-	12 A @ 100 V AC 6 A @ 240 V AC	-
Chassis +3.3 V Current	-	-	20 A	Maximum combined power at 3.3 and 5 V rails is 150 W.
Chassis +5 V Current	-	-	20 A	
Chassis +12 V Current	-	-	83.3 A	Maximum power at 12 V rail is 1000 W.
Chassis +5 VSB Current	-	-	3 A	Maximum power at 5 VSB rail is 15 W.
Chassis -12 V Current	-	-	1 A	-
Chassis Total Power	-	-	1000 W	-
System Controller Slot Current Capability	-	-	30 A 15 A 15 A 3 A -	From +12 V From +5 V From +3.3 V From +5 VSB From -12 V
Hybrid Peripheral Slot Current Capability	-	-	6 A 9 A 9 A 1 A 1 A	From +12 V From +5 V From +3.3 V From +5 VSB From -12 V
PXI Express Slot Current Capability	-	-	6 A 9 A 9 A 1 A -	From +12 V From +5 V From +3.3 V From +5 VSB From -12 V
Number of Hybrid Slots	-	9	-	-
Number of PXIe Slots	-	0	-	All slots are hybrid.
System Timing Slot	-	0	-	No system timing slot.
Slot Count	-	10	-	-
Slot Cooling Capacity	-	-	82 W	-
System Bandwidth	-	-	16 GB/s	-
PCIe Version	-	Gen 3	-	-
PXIe Link Capacity	-	4 Link	-	-
PCI Bit Count	-	32 bit	-	-
PCI Frequency	-	33 MHz or 66 Mhz	-	-

2.2.2. Clock

DE140000 has an internal clock structure that generates required clock and synchronization signals.

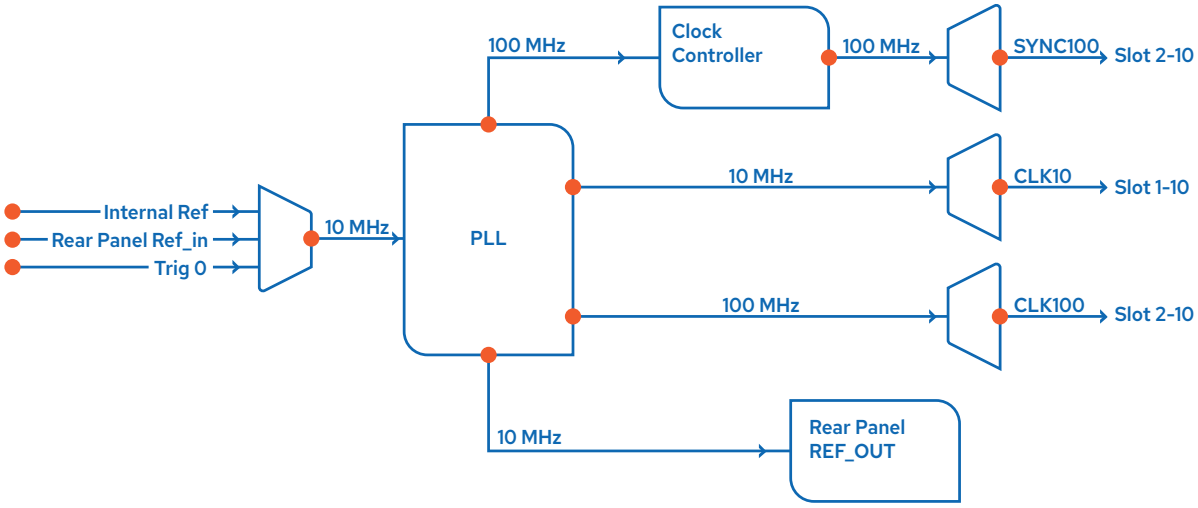

Figure 2: Chassis Clock Structure

Clock source can be selected via programming through SMBus. The source can be selected as an internal clock, or an external clock from rear panel, or an external clock from Trig 0 port. PXI CLK10, CLK100 and SYNC100 is phase locked to the selected clock source.

2.2.3. Power Modes

The chassis has different power supply activation modes.

Table 2: Power Supply Operating Modes

Rear Panel INHIBIT MODE Switch	System Controller Presence	Power Supply Behavior
Manual	-	Directly connected to INHIBIT_N button. (Power active at LOW)
Default	Present	Normal ATX operation when power button pressed.
Default	Absent	If power button pressed for 4 seconds when the power off, power is activated. If power button pressed for 4 seconds when the power on, power is deactivated.

2.2.4. Physical

Table 3: Physical Specifications

Specification	Description
Dimensions (L / W)	355.4 mm x 355.5 mm
Height (H)	177 + 47 mm
Rear Panel Connector	2 row DSUB15, ASSMANN: AB420
REF_IN, REF_OUT Connector	BNC, AMPHENOL: 112132

2.2.5. Environmental

Table 4: Environmental Specifications

Specification	Condition	Value
Operating Humidity	Relative, non-condensing	10% - 90%
Storage Humidity	Relative, non-condensing	5% - 95%
Operating Temperature	Forced-air cooling from chassis	0 °C - +40 °C
Storage Temperature	-	-40 °C – +71 °C

3. Software Overview

This device is PXI Express compatible.

4. Signal Connections

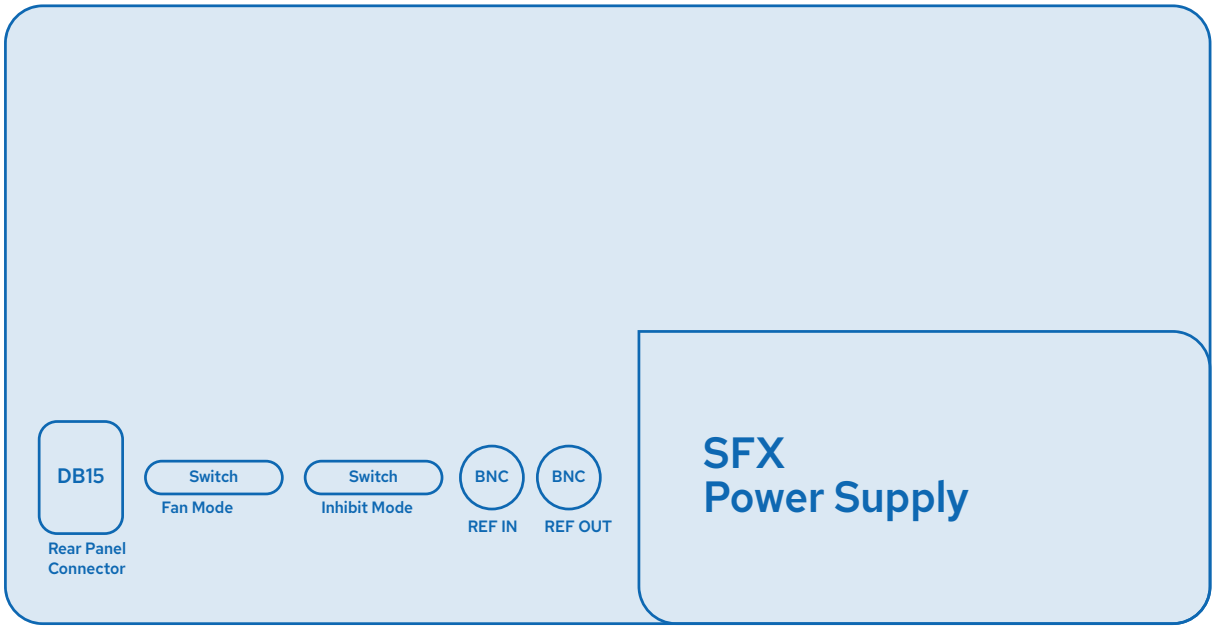

Figure 3: DE140000 Connector Interface

4.1. Rear Panel Connector

Analog bus interface is carried to the outside with the standard DSUB15 (ASSMANN PN: AB420) connector. Mating connector can be selected among any 2 row DSUB15 male connector.

Table 5: Rear Panel Connector Pinout

Pin	Pin Description	Function
1	GND	GND
2	P5V0	P5V0 voltage monitor
3	FAULT_REAR	Rear panel power fault indicator output (H: power fault) (L: power OK)
4	P3V3	P3V3 voltage monitor
5	INHIBIT_N	Rear panel power inhibit input (active low)
6	P12V0	P12V0 voltage monitor
7	NC	Not connected
8	N12V0	N12V0 voltage monitor
9	GND	GND
10	PFI3	Programmable function interface 3
11	PFI2	Programmable function interface 2
12	GND	GND
13	PFI1	Programmable function interface 1
14	PFI0	Programmable function interface 0
15	GND	GND

Table 6: Fault Output Signal Specifications

Specification	Value
V_{OH}	2.4 V min
V_{OL}	0.4 V max

Table 7: PFI Signal Specifications

Specification	Value
V_{IH}	2 V min
V_{IL}	0.8 V max
V_{OH}	2.4 V min
V_{OL}	0.8 V max

4.2. Fan Mode Switch

Fan mode can be selected by a rear panel switch.

Table 8: Fan Operation Modes

Mode	Function
Auto	Auto fan speed applied according to the temperature sensors.
Max	Maximum fan speed applied.

4.3. Inhibit Mode Switch

Inhibit mode can be selected by a rear panel switch.

Table 9: Inhibit Mode Options

Mode	Function
Default	Internal configurations are applied for power supply activation.
Manual	Manual power supply activation from rear panel INHIBIT_N pin is enabled.

Table 10: Inhibit Input Signal Specifications

Specification	Value
V_{IH}	2.4 V min
V_{IL}	1 V max

4.4. REF_IN and REF_OUT

10 MHz reference clock input and output interfaces are placed at rear panel.

Table 11: Reference Clock Interfaces

Connector	Function
REF_IN	10 MHz clock input. It can be used as reference clock input for the chassis clock structure.
REF_OUT	10 MHz clock output. Output clock can be enabled and disabled from system controller.

Table 12: REF_OUT Specifications

Specification	Value
Accuracy	±25 ppm max
Maximum Jitter	5 ps RMS phase-jitter
Output Amplitude	1.65 Vpp ±20% square-wave into 50 Ω, 3.3 Vpp unloaded
Output Inpedence	50 Ω ±5 Ω

Table 13: REF_IN Specifications

Specification	Value
Frequency	10 MHz ±25 ppm
Input Amplitude	100 mVpp to 5 Vpp square-wave or sine-wave
Maximum Jitter	1 ps RMS phase-jitter
Rear Panel BNC Input Impedance	50 Ω ±5 Ω

5. Configuration

DE140000 can work with any PXIe System Controller Module, PXIe Peripheral Module and CPCI Module. The modules should be slid inside the DE140000.

Figure 4: DE140000 and a Related Module Configuration

6. Safety Guidelines

Caution

The DE140000 shall not be operated in any manner not specified in this document. Misuse of the product may result in a hazard. Safety protection features may be compromised if the product is damaged. In the event of damage, the product shall be returned for repair.

7. Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC). These requirements and limits provide reasonable protection against harmful interference when the product is operated in the intended operational electromagnetic environment.

This product is intended for use in industrial locations. However, harmful interference may occur in some installations, if the product is connected to a peripheral device or test object, or if the product is used in residential or commercial areas. To minimize interference with radio and television reception and prevent unacceptable performance degradation, install and use this product in strict accordance with the instructions specified in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by DEICO could void your authority to operate it under your local regulatory rules.

Caution

To ensure the specified EMC performance, the product shall be operated only with shielded cables and accessories.

Caution

To ensure the specified EMC performance, the length of any cable attached to front connectors must not be longer than 3 m (10 ft.).

8. Supporting Products & Software

DE140000 could be used with related modules.

support@**deico.com.tr**
+90 312 395 68 44