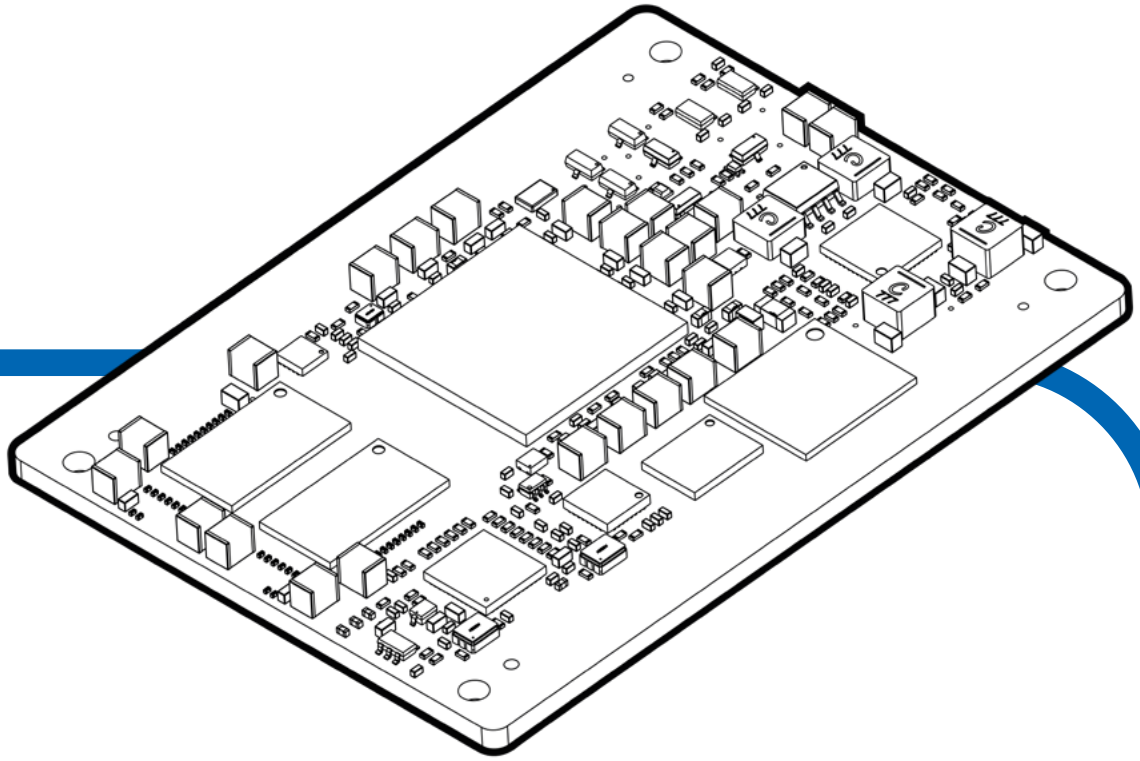
Datasheet



DE13210

Zynq-7015 System on Module (SoM)

DEICO

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Contents

1. Description

DE13210 Zynq-7015 System on Module (SoM) is an embedded core board which uses Xilinx Zynq-7000 series XC7Z015 SoC FPGA with dual core ARM® Cortex™-A9 based processing system. The SoM is very compact and includes fundamental components such as DDR Memory, QSPI Flash, eMMC, USB PHY and Ethernet PHY. The SoM offers rapid designs and design flexibility.

1.1. Key Features

- Zynq-7000 Series SoC FPGA (XC7Z015)
- Small form factor
- 1 GB DDR3 SDRAM
- 8 GB eMMC
- 32 MB QSPI flash
- 2 KB EEPROM
- 10/100/1000 Mb/s Ethernet PHY
- USB 2.0 PHY
- Temperature sensor
- 137 PL I/O (66 differential pairs)
- 21 PS I/O
- 4-lane PL GTP transceivers
- Adjustable PL I/O voltage

2. Hardware Overview

2.1. SoC

- Dual-core ARM Cortex-A9 MPCore™ with CoreSight™
- 8 DMA channels
- 2x AXI 32-bit master 2x AXI 32-bit slave
- 4x AXI 64-bit/32-bit memory
- 16 interrupt

2.2. Peripherals

- 10/100/1000 Mb/s Ethernet PHY
- USB PHY *
- 2× UART *
- 2× I²C *
- 2× CAN bus *
- 2× SPI *
- 137 PL I/Os (66 differential pairs)
- 21 PS I/Os
- 4-lane PL GTP transceivers

*Protocols can implement in PS but they can use PL pins.

2.3. Circuitry

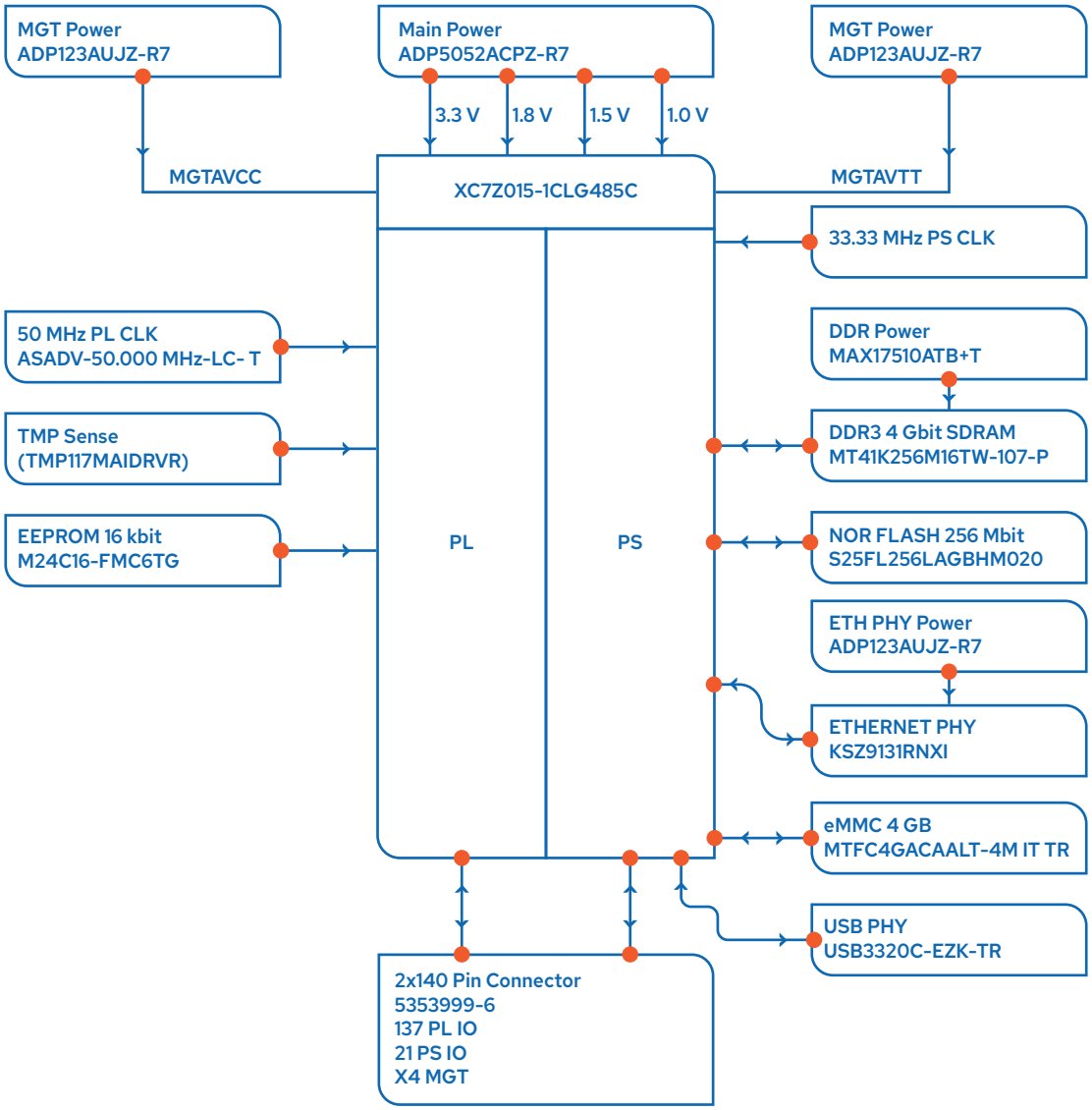

Figure 1: Block Diagram of SoM

2.4. Hardware Specifications

2.4.1. DDR Memory

The SoM includes 2 x 4 Gbit DDR3 RAM with part number MT41K256M16TW-107-P. DDR3 RAMs are connected to PS dedicated DDR3 pins of Zynq-SoC. DDR3 RAM schematic is given in Figure 2.

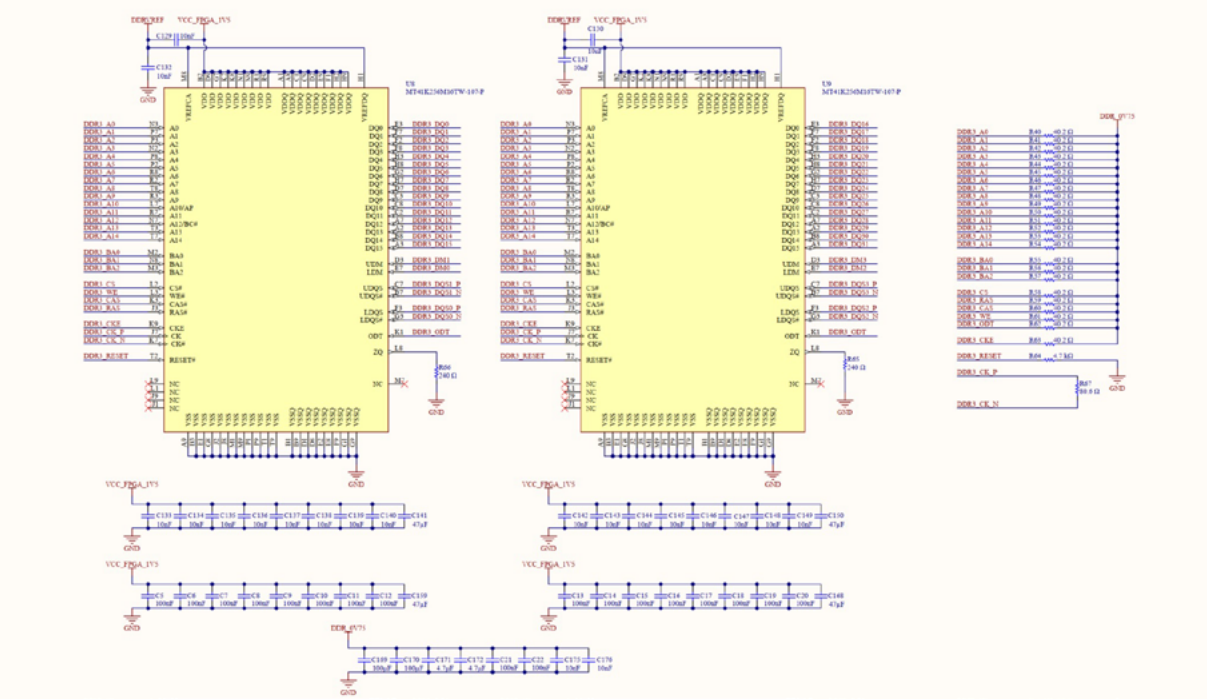

Figure 2: DDR3 RAM

2.4.2. Quad-SPI Flash Memory

The SoM includes 256 kbit Quad-SPI Flash memory with part number S25FL256LAGBHM020. This QSPI can be used to initialize the FPGA with bitstream. QSPI Flash Memory schematic is given in Figure 3. QSPI Memory FPGA connection is given in Table 1.

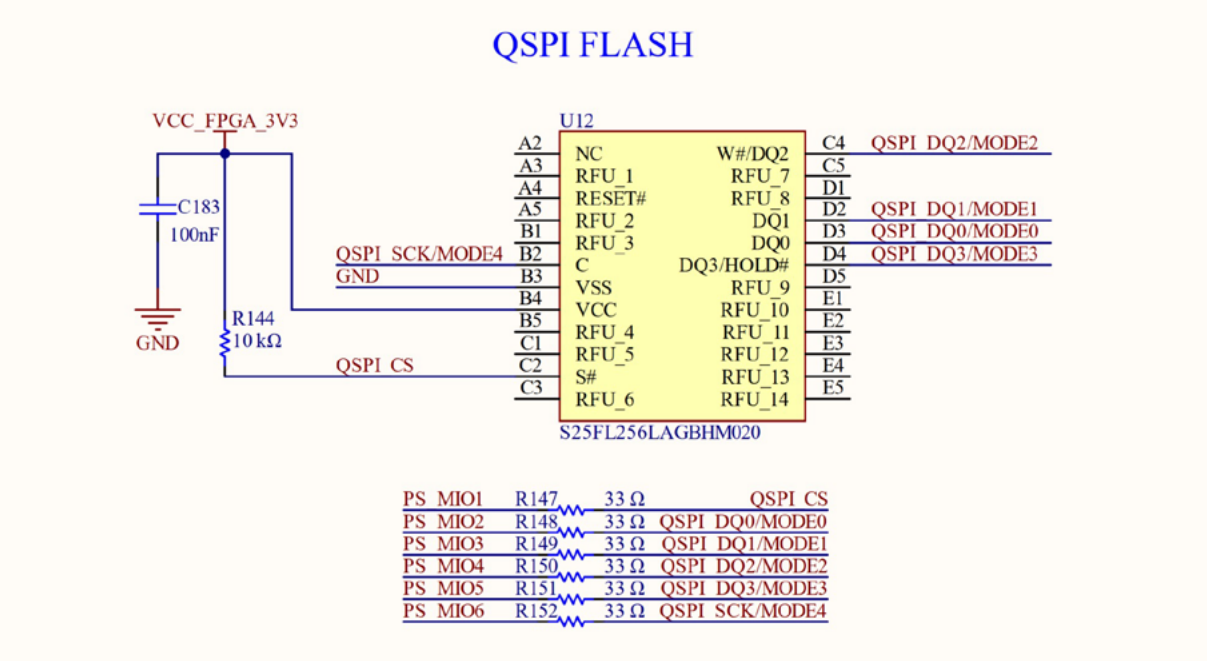

Figure 3: QSPI Flash

Table 1: QSPI Connection

Signal	Bank	Pin	Ball
QSPI_CS	BANK500	MIO1	A22
QSPI_DQ0/MODE0	BANK500	MIO2	A21
QSPI_DQ1/MODE1	BANK500	MIO3	F17
QSPI_DQ2/MODE2	BANK500	MIO4	E19
QSPI_DQ3/MODE3	BANK500	MIO5	A20
QSPI_SCK/MODE4	BANK500	MIO6	A19

2.4.3. eMMC Memory

The SoM includes 8 GB eMMC memory with part number MTFC8GAMALBH-AAT. eMMC is connected to PS dedicated SD1 MIO pins. eMMC memory schematic is given in Figure 4. eMMC FPGA connection is given in Table 2.

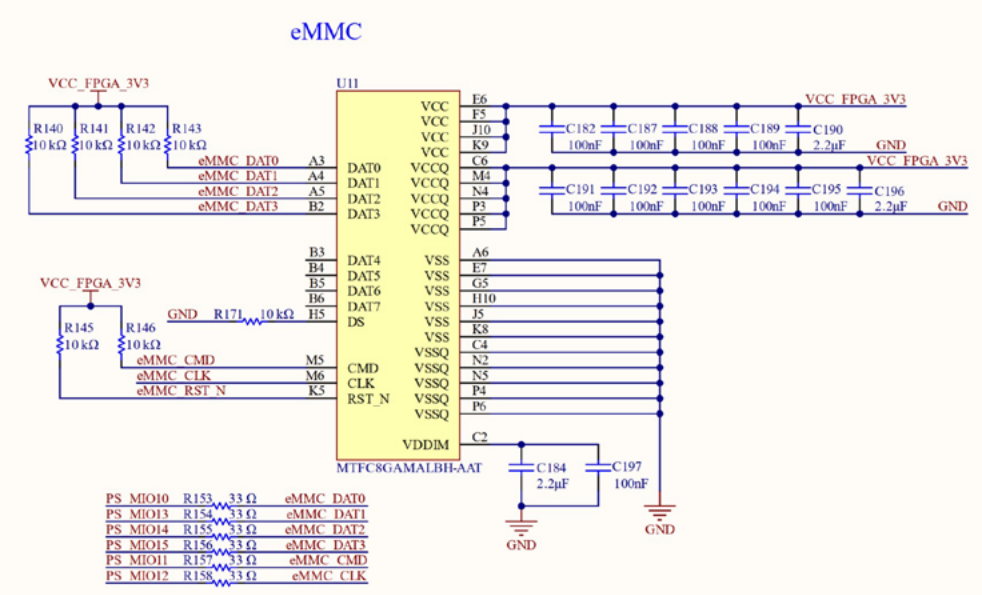

Figure 4: eMMC Memory

Table 2: eMMC Connection

Signal	Bank	Pin	Ball
eMMC_DAT0	BANK500	MIO10	G16
eMMC_DAT1	BANK500	MIO13	A17
eMMC_DAT2	BANK500	MIO14	B17
eMMC_DAT3	BANK500	MIO15	E17
eMMC_CMD	BANK500	MIO11	B19
eMMC_CLK	BANK500	MIO12	C18

2.4.4. EEPROM

The SoM includes 16 kbit EEPROM with part number M24C16-FMC6TG. EEPROM schematic is given in Figure 5. EEPROM FPGA connection is given in Table 3.

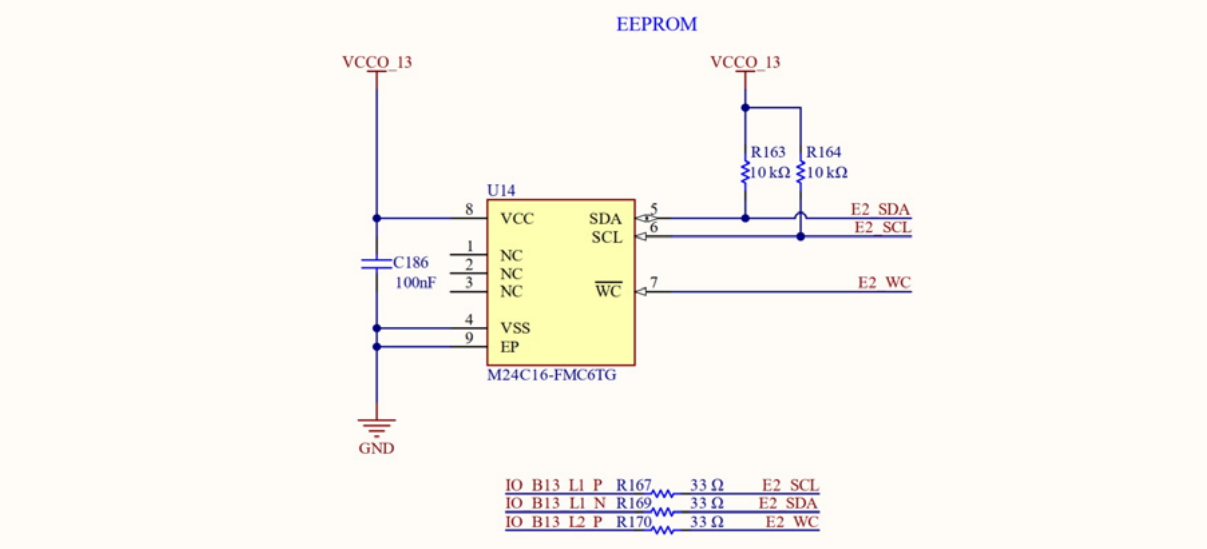

Figure 5: EEPROM

Table 3: EEPROM Connection

Signal	Bank	Pin	Ball
E2_SCL	BANK13	IO_B13_L1_P	V13
E2_SDA	BANK13	IO_B13_L1_N	V14
E2_WC	BANK13	IO_B13_L2_P	V15

2.4.5. 10/100/1000 Mb/s Ethernet PHY

The SoM includes 10/100/1000 Mb/s Ethernet PHY with part number KSZ9131RNXI. KSZ9131RNXI is a RGMII to ethernet PHY. RGMII pins are connected to PS dedicated GEM0 MIO pins. Ethernet PHY schematic is given in Figure 6. Ethernet PHY FPGA connection is given in Table 4.

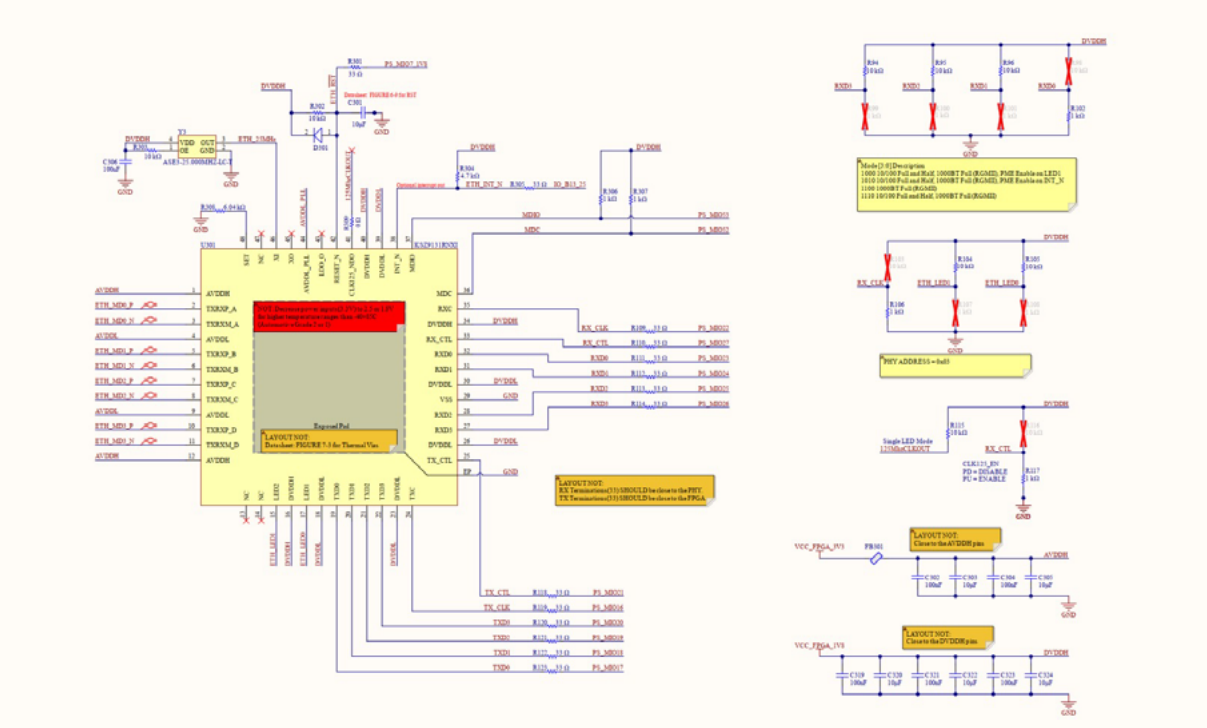

Figure 6: Ethernet PHY

Table 4: Ethernet PHY Connection

Signal	Bank	Pin	Ball
TX_CLK	BANK501	MIO16	D17
TXD0	BANK501	MIO17	E14
TXD1	BANK501	MIO18	A16
TXD2	BANK501	MIO19	E13
TXD3	BANK501	MIO20	A15
TX_CTL	BANK501	MIO21	F12
RX_CLK	BANK501	MIO22	A9
RXD0	BANK501	MIO23	E12
RXD1	BANK501	MIO24	B16
RXD2	BANK501	MIO25	F11
RXD3	BANK501	MIO26	A10
RX_CTL	BANK501	MIO27	D16
MDC	BANK501	MIO52	D13
MDIO	BANK501	MIO53	C11

2.4.6. USB PHY

The SoM includes USB PHY with part number USB3320C-EZK-TR. USB3320C-EZK-TR is a USB PHY which supports OTG. USB PHY pins are connected to PS dedicated MIO pins. USB PHY schematic is given in Figure 7. Ethernet PHY FPGA connection is given in Table 5.

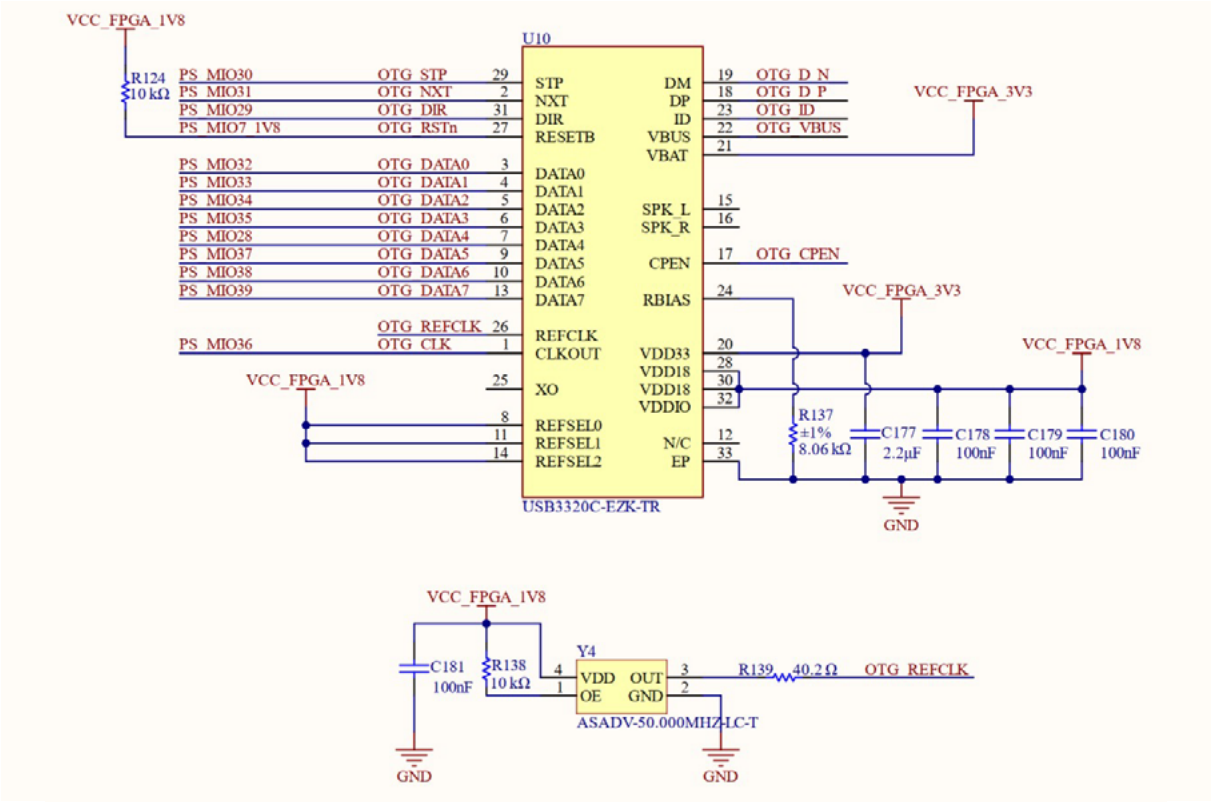

Figure 7: USB PHY

Table 5: USB PHY Connection

Signal	Bank	Pin	Ball
OTG_DIR	BANK501	MIO29	D17
OTG_STP	BANK501	MIO30	E14
OTG_NXT	BANK501	MIO31	A16
OTG_DATA0	BANK501	MIO32	E13
OTG_DATA1	BANK501	MIO33	A15
OTG_DATA2	BANK501	MIO34	F12
OTG_DATA3	BANK501	MIO35	A9
OTG_DATA4	BANK501	MIO28	E12
OTG_DATA5	BANK501	MIO37	B16
OTG_DATA6	BANK501	MIO38	F11
OTG_DATA7	BANK501	MIO39	A10
OTG_CLK	BANK501	MIO36	D16

2.4.7. Temperature Sensor

The SoM includes a temperature sensor with part number TMP117MAIDRVR. Temperature sensor schematic is given in Figure 8. Temperature sensor FPGA connection is given in Table 6.

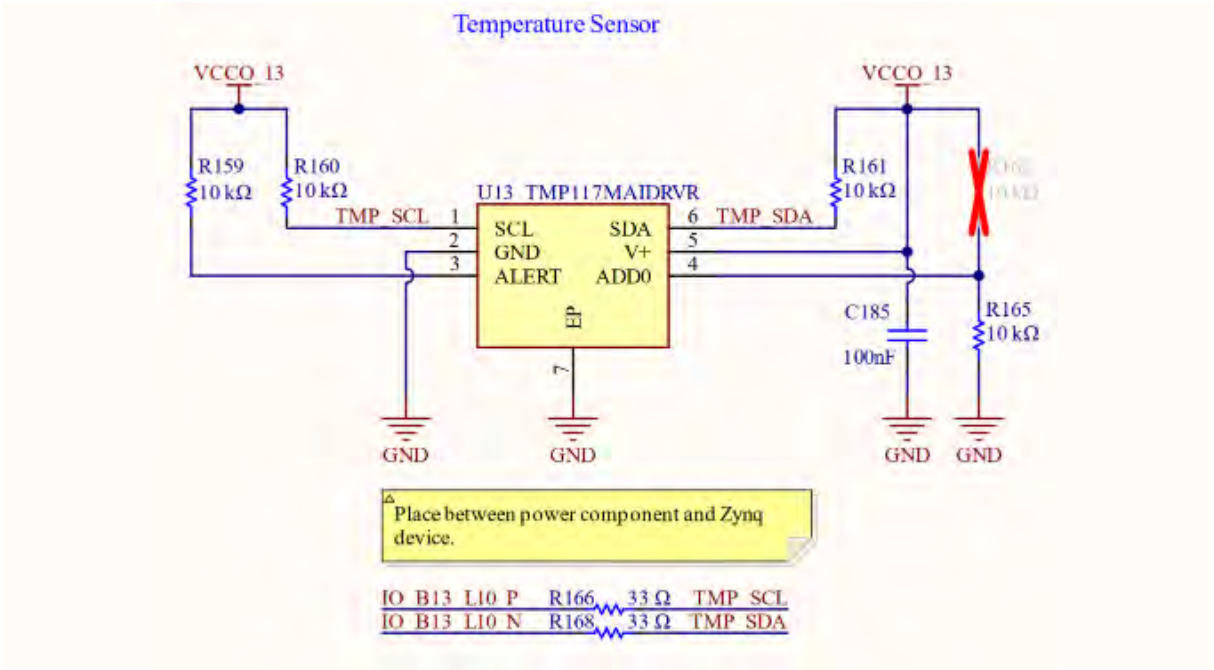

Figure 8: Temperature Sensor

Table 6: Temperature Sensor Connection

Signal	Bank	Pin	Ball
TMP_SCL	BANK13	IO_B13_L10_P	Y12
TMP_SDA	BANK13	IO_B13_L10_N	Y13

2.5. Electrical

The SoM needs a 5 V power for the SoM general power supply. Further, the SoM needs power supply for the bank voltages. Bank voltages can be supplied from a single power supply or can be adjusted to different voltage levels with separate power supplies. Power supply requirements are given in Table 1. Zynq-7000 SoC DC and AC Switching Characteristics (DS187) should be referred to for more information on bank voltages and IO electrical characteristic.

Table 7: Power Requirements of SoM

Parameter	Min	Typ	Max	Units
VCC_5V0	4.75	5	5.25	V
Supply Current of VCC_5V0 (Idle)	–	–	800	mA
Supply Current of VCC_5V0 (In full operation)	–	–	2000	mA
Bank Voltages (BANK12, BANK34, BANK35)	1.8	–	3.3	V
Supply Current of Bank Powers	–	–	300	mA

2.6. Physical

Physical dimensions of the SoM are given in Figure 9, Figure 10 and Figure 11.

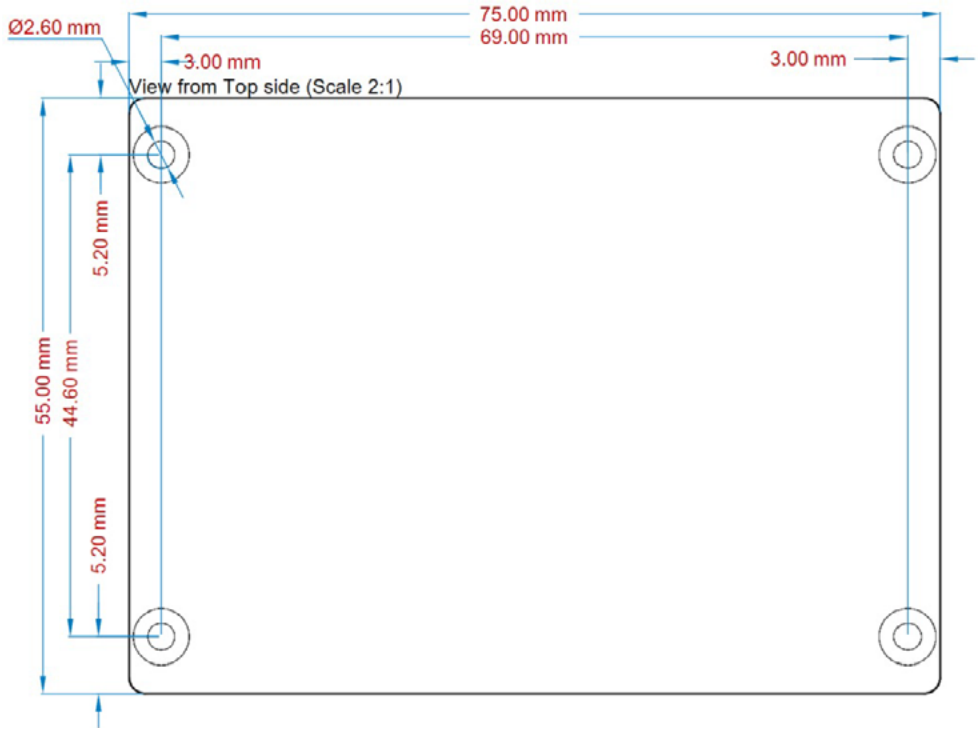

Figure 9: Top Side Dimensions

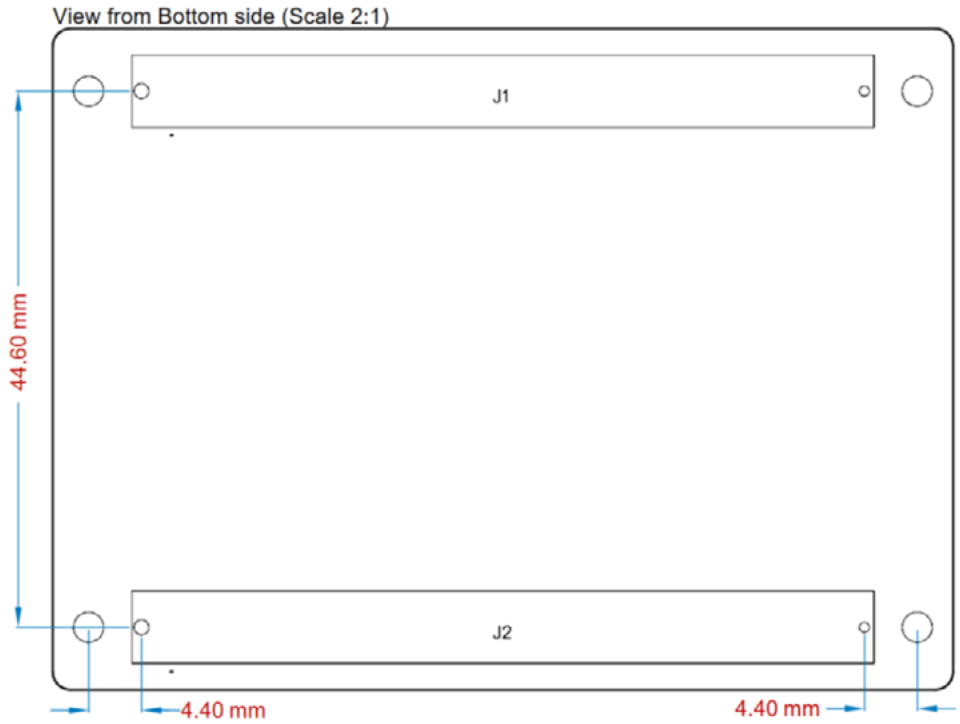

Figure 10: Bottom Side Dimensions

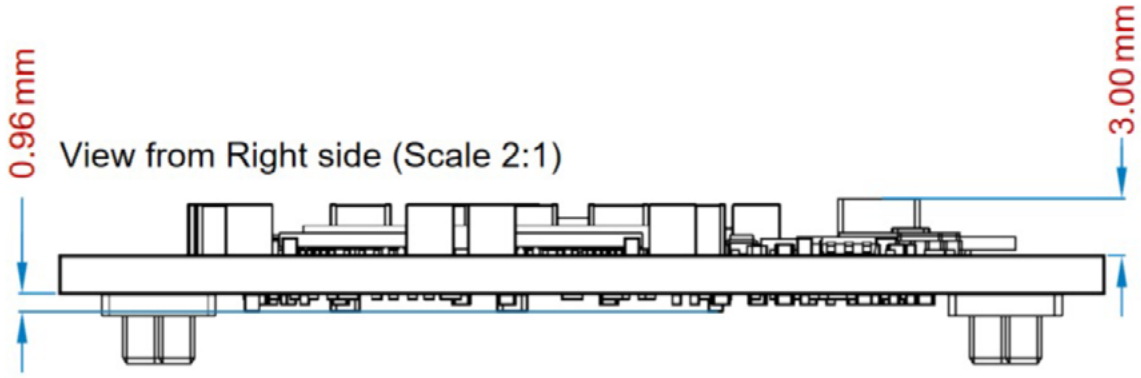

Figure 11: Right Side Dimensions

2.7. Environmental

The SoM environmental specifications are given in Table 8.

Table 8: Environmental Specificatons

Parameter	Condition	Value
Operating Humidity	Relative, non-condensing	10%- 90%
Storage Humidity	Relative, non-condensing	5%- 95%
Operating Temperature	Forced-air cooling from chassis	0 °C - 40 °C
Storage Temperature	–	0 °C - 70 °C

3. Signal Connections

The SoM connectors and their matings are given in Table 9.

Table 9: J1 & J2 Connector

Connector	MFG NO	MFG
J1 & J2 Connector	5177983-6	TE Connectivity
J1 & J2 Connector Mating	5177984-6	TE Connectivity

The SoM J1 connector pinout is given in Table 10.

Table 10: J1 Connector Pinout

Signal	Bank	Ball	Pin	Pin	Ball	Bank	Signal
VCC_5V0			1	2			VCC_5V0
VCC_5V0			3	4			VCC_5V0
GND			5	6			GND
ETH_MD0_P			7	8			GND
ETH_MD0_N			9	10			ETH_MD1_P
GND			11	12			ETH_MD1_N
ETH_MD2_P			13	14			GND

Signal	Bank	Ball	Pin	Pin	Ball	Bank	Signal
ETH_MD2_N			15	16			ETH_MD3_P
GND			17	18			ETH_MD3_N
OTG_D_P			19	20			GND
OTG_D_N			21	22	D13	BANK501	PS_MIO52
GND			23	24	C11	BANK501	PS_MIO53
OTG_ID			25	26			ETH_LED0
OTG_VBUS			27	28			ETH_LED1
IO_B35_0	BANK35	H6	29	30			OTG_CPEN
IO_B35_L3_P	BANK35	E8	31	32			GND
IO_B35_L3_N	BANK35	D8	33	34	G8	BANK35	IO_B35_L4_P
IO_B35_L7_P	BANK35	C8	35	36	G7	BANK35	IO_B35_L4_N
IO_B35_L7_N	BANK35	B8	37	38	F7	BANK35	IO_B35_L1_P
IO_B35_L6_P	BANK35	G6	39	40	E7	BANK35	IO_B35_L1_N
IO_B35_L6_N	BANK35	F6	41	42	D5	BANK35	IO_B35_L12_P
GND			43	44	C4	BANK35	IO_B35_L12_N
IO_B35_L10_P	BANK35	A5	45	46			GND
IO_B35_L10_N	BANK35	A4	47	48	B4	BANK35	IO_B35_L13_P
IO_B35_L8_P	BANK35	B7	49	50	B3	BANK35	IO_B35_L13_N
IO_B35_L8_N	BANK35	B6	51	52	D3	BANK35	IO_B35_L14_P
GND			53	54	C3	BANK35	IO_B35_L14_N
IO_B35_L11_P	BANK35	C6	55	56	F5	BANK35	IO_B35_L5_P
IO_B35_L11_N	BANK35	C5	57	58	E5	BANK35	IO_B35_L5_N
VCCO_BANK35			59	60			VCCO_BANK35
GND			61	62			GND
IO_B35_L9_P	BANK35	A7	63	64	G4	BANK35	IO_B35_L20_P
IO_B35_L9_N	BANK35	A6	65	66	F4	BANK35	IO_B35_L20_N
IO_B35_L2_P	BANK35	D7	67	68	D1	BANK35	IO_B35_L16_P
IO_B35_L2_N	BANK35	D6	69	70	C1	BANK35	IO_B35_L16_N
IO_B35_L15_P	BANK35	A2	71	72	E2	BANK35	IO_B35_L17_P
IO_B35_L15_N	BANK35	A1	73	74	D2	BANK35	IO_B35_L17_N
GND			75	76			GND
IO_B35_L18_P	BANK35	B2	77	78	E4	BANK35	IO_B35_L21_P
IO_B35_L18_N	BANK35	B1	79	80	E3	BANK35	IO_B35_L21_N
GND			81	82	G3	BANK35	IO_B35_L22_P
IO_B35_L23_P	BANK35	F2	83	84	G2	BANK35	IO_B35_L22_N
IO_B35_L23_N	BANK35	F1	85	86	H4	BANK35	IO_B35_L19_P
IO_B35_L24_P	BANK35	H1	87	88	H3	BANK35	IO_B35_L19_N
IO_B35_L24_N	BANK35	G1	89	90	H5	BANK35	IO_B35_25
GND			91	92			GND
XADC_VCC		K12	93	94	H11	BANK0	TCK
XADC_IN0_P		L12	95	96	H10	BANK0	TMS
XADC_IN0_N		M11	97	98	H9	BANK0	TDI
XADC_TMP_P		N12	99	100	G9	BANK0	TDO
XADC_TMP_N		N11	101	102			GND
XADC_GND		K11	103	104	E9	BANK501	PS_MIO40
GND			105	106	C15	BANK501	PS_MIO41

Signal	Bank	Ball	Pin	Pin	Ball	Bank	Signal
PS_MIO0	BANK500	G17	107	108	D15	BANK501	PS_MIO42
PS_MIO2	BANK500	A21	109	110	B12	BANK501	PS_MIO43
PS_MIO4	BANK500	E19	111	112	E10	BANK501	PS_MIO44
PS_MIO8	BANK500	E18	113	114	B14	BANK501	PS_MIO45
PS_MIO9	BANK500	C19	115	116	B13	BANK501	PS_MIO46
PS_MIO3	BANK500	F17	117	118	D11	BANK501	PS_MIO47
PS_MIO5	BANK500	A20	119	120			GND
PS_MIO6	BANK500	A19	121	122	D12	BANK501	PS_MIO48
			123	124	C9	BANK501	PS_MIO49
			125	126	D10	BANK501	PS_MIO50
			127	128	C13	BANK501	PS_MIO51
GND			129	130	T8	BANK0	FPGA_INIT
System_PG			131	132	V10	BANK0	PROGRAM_B_0
PS_MIO7	BANK500	D18	133	134	T10	BANK0	FPGA_DONE
PS_RST	BANK501	C14	135	136	G14	BANK0	VCCBATT
			137	138			VCCO_501
VCCO_500			139	140			GND

The SoM J2 connector pinout is given in Table 11.

Table 11: J2 Connector Pinout

Signal	Bank	Ball	Pin	Pin	Ball	Bank	Signal
VCC_5V0			1	2			VCC_5V0
VCC_5V0			3	4			VCC_5V0
GND			5	6			GND
IO_B34_25	BANK34	R8	7	8	H8	BANK34	IO_B34_0
IO_B34_L16_P	BANK34	N1	9	10	J8	BANK34	IO_B34_L1_P
IO_B34_L16_N	BANK34	P1	11	12	K8	BANK34	IO_B34_L1_N
IO_B34_L19_P	BANK34	N6	13	14	K7	BANK34	IO_B34_L3_P
IO_B34_L19_N	BANK34	N5	15	16	L7	BANK34	IO_B34_L3_N
IO_B34_L12_P	BANK34	L5	17	18	J7	BANK34	IO_B34_L2_P
IO_B34_L12_N	BANK34	L4	19	20	J6	BANK34	IO_B34_L2_N
GND			21	22			GND
IO_B34_L18_P	BANK34	P3	23	24	J5	BANK34	IO_B34_L7_P
IO_B34_L18_N	BANK34	P2	25	26	K5	BANK34	IO_B34_L7_N
IO_B34_L11_P	BANK34	K4	27	28	M8	BANK34	IO_B34_L6_P
IO_B34_L11_N	BANK34	K3	29	30	M7	BANK34	IO_B34_L6_N
IO_B34_L13_P	BANK34	T2	31	32	N8	BANK34	IO_B34_L5_P
IO_B34_L13_N	BANK34	T1	33	34	P8	BANK34	IO_B34_L5_N
VCCO_BANK34			35	36			VCCO_BANK34
GND			37	38			GND
IO_B34_L10_P	BANK34	L2	39	40	P7	BANK34	IO_B34_L24_P
IO_B34_L10_N	BANK34	L1	41	42	R7	BANK34	IO_B34_L24_N
IO_B34_L15_P	BANK34	M2	43	44	R5	BANK34	IO_B34_L23_P
IO_B34_L15_N	BANK34	M1	45	46	R4	BANK34	IO_B34_L23_N
IO_B34_L8_P	BANK34	J2	47	48	P6	BANK34	IO_B34_L20_P
IO_B34_L8_N	BANK34	J1	49	50	P5	BANK34	IO_B34_L20_N

Signal	Bank	Ball	Pin	Pin	Ball	Bank	Signal
GND			51	52			GND
IO_B34_L22_P	BANK34	M4	53	54	R3	BANK34	IO_B34_L17_P
IO_B34_L22_N	BANK34	M3	55	56	R2	BANK34	IO_B34_L17_N
IO_B34_L9_P	BANK34	J3	57	58	N4	BANK34	IO_B34_L21_P
IO_B34_L9_N	BANK34	K2	59	60	N3	BANK34	IO_B34_L21_N
IO_B34_L4_P	BANK34	L6	61	62	U2	BANK34	IO_B34_L14_P
IO_B34_L4_N	BANK34	M6	63	64	U1	BANK34	IO_B34_L14_N
GND			65	66			GND
IO_B13_L15_P	BANK13	AB21	67	68	Y18	BANK13	IO_B13_L13_P
IO_B13_L15_N	BANK13	AB22	69	70	Y19	BANK13	IO_B13_L13_N
IO_B13_L16_P	BANK13	AB18	71	72	V18	BANK13	IO_B13_L21_P
IO_B13_L16_N	BANK13	AB19	73	74	W18	BANK13	IO_B13_L21_N
IO_B13_L18_P	BANK13	AA19	75	76	AA16	BANK13	IO_B13_L14_P
IO_B13_L18_N	BANK13	AA20	77	78	AA17	BANK13	IO_B13_L14_N
GND			79	80			GND
VCCO_BANK13			81	82			VCCO_BANK13
IO_B13_L17_P	BANK13	AB16	83	84	T16	BANK13	IO_B13_0
IO_B13_L17_N	BANK13	AB17	85	86	U19	BANK13	IO_B13_L20_P
IO_B13_L22_P	BANK13	U17	87	88	V19	BANK13	IO_B13_L20_N
IO_B13_L22_N	BANK13	U18	89	90	AA14	BANK13	IO_B13_L11_P
IO_B13_L23_P	BANK13	V16	91	92	AA15	BANK13	IO_B13_L11_N
IO_B13_L23_N	BANK13	W16	93	94	AB13	BANK13	IO_B13_L9_P
GND			95	96	AB14	BANK13	IO_B13_L9_N
IO_B13_L19_P	BANK13	R17	97	98			GND
IO_B13_L19_N	BANK13	T17	99	100	AA11	BANK13	IO_B13_L7_P
IO_B13_L3_P	BANK13	W12	101	102	AB11	BANK13	IO_B13_L7_N
IO_B13_L3_N	BANK13	W13	103	104	U11	BANK13	IO_B13_L5_P
IO_B13_L8_P	BANK13	AA12	105	106	U12	BANK13	IO_B13_L5_N
IO_B13_L8_N	BANK13	AB12	107	108	V11	BANK13	IO_B13_L4_P
GND			109	110	W11	BANK13	IO_B13_L4_N
MGTP_TX0_P		AA3	111	112			GND
MGTP_TX0_N		AB3	113	114	AA5		MGTP_TX2_P
GND			115	116	AB5		MGTP_TX2_N
MGTP_RX0_P		AA7	117	118			GND
MGTP_RX0_N		AB7	119	120	AA9		MGTP_RX2_P
GND			121	122	AB9		MGTP_RX2_N
MGTP_TX1_P		W4	123	124			GND
MGTP_TX1_N		Y4	125	126	W2		MGTP_TX3_P
GND			127	128	Y2		MGTP_TX3_N
MGTP_RX1_P		W8	129	130			GND
MGTP_RX1_N		Y8	131	132	W6		MGTP_RX3_P
GND			133	134	Y6		MGTP_RX3_N
MGTREF_CLK0_P		U9	135	136			GND
MGTREF_CLK0_N		V9	137	138	U5		MGTREF_CLK1_P
GND			139	140	V5		MGTREF_CLK1_N

4. Configuration

All configuration pins should be connected to the carrier board. The SoM can be configured in all boot modes. Boot mode options are given in Table 6. Zynq-7000 SoC Technical Reference Manual (UG585) section 6: Boot and Configuration should be referred to for more information.

Table 12: Boot Mode

Pin-Signal / Mode	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]	
	BOOT_ MODE[4]	BOOT_ MODE[0]	BOOT_ MODE[2]	BOOT_ MODE[1]	BOOT_MODE[3]	
Boot Devices						
JTAG Boot Mode		0	0	0		
NOR Boot		0	0	1		JTAG Chain Routing
NAND		0	1	0		0: Cascade Mode 1: Independent Mode
Quad-PI		1	0	0		
SD-Card		1	1	0		
Mode for all PLLs						
PLL Enabled	0	Hardware waits for PLL to lock, then executes BootROM.				
PLL Bypassed	1	Allows for a wide PS_CLK frequency range.				